NEC

TFT COLOR LCD MODULE

Type No. NL128102AC31-01

51cm (20.1Type), SXGA

Analog, Full-color

First edition

DATA SHEET

All information in this document are subject to change without prior notice.

NEC Corporation
Display Device Operations Unit
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Contents

1. DESCRIPTION

NL128102AC31-01 is a TFT(thin film transistor) active matrix color liquid crystal display (LCD) comprising amorphous silicon TFT attached to each signal electrode, a driving circuit and a backlight. NL128102AC31-01 has a built-in backlight with an inverter.

The 51cm(20.1 type) diagonal display area contains 1280×1024 pixels and can display full color (more than 16 million colors simultaneously). Also, it has ultra-wide view angle and multi-scan function. Therefore, this module calls Super Fine TFT.

2. FEATURES

- Ultra wide viewing angle
- Large display size
- Analog RGB interface
- Multi-scan function: e.g., SXGA, XGA, MAC, SVGA, VGA, PC9801, VGA-TEXT, PAL, NTSC
- Low reflection
- High luminance
- Incorporated direct type backlight(Ten cold cathode fluorescent lamps, inverter)
- Lamp unit replaceable(Type No.:201LHS01)

3. APPLICATIONS

- Monitor
- Engineering workstation (EWS)
- Personal computer (PC)

4. STRUCTURE AND FUNCTIONS

A color TFT (thin film transistor) LCD module is comprised of a TFT liquid crystal panel structure, LSIs for driving the TFT array, and a backlight assembly. The TFT panel structure is created by sandwiching liquid crystal material in the narrow gap between a TFT array glass substrate and a color filter glass substrate. After the driver LSIs are connected to the panel, the backlight assembly is attached to the backside of the panel.

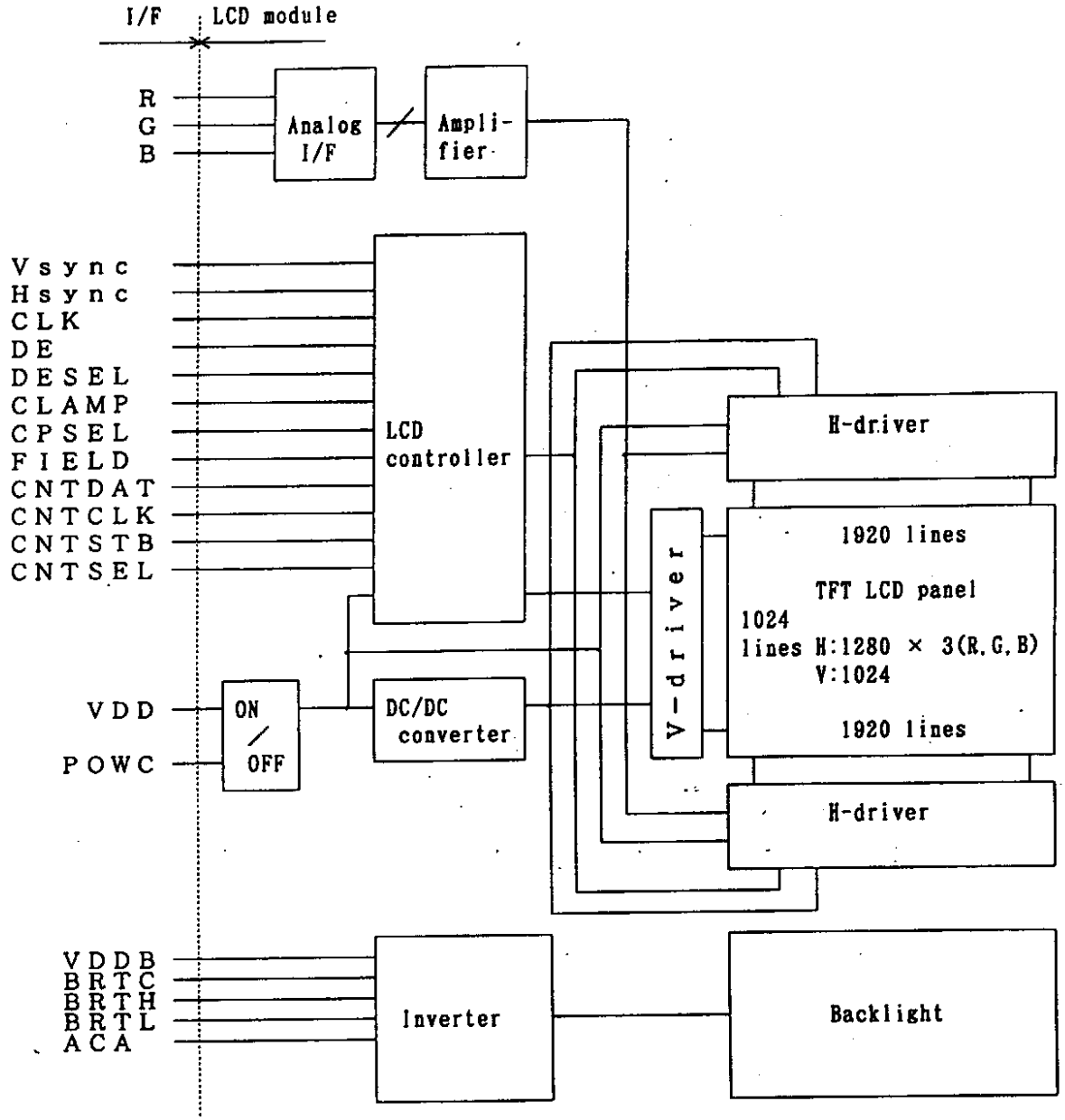
RGB (red, green, blue) data signals from a source system is modulated into a form suitable for active matrix addressing by the onboard signal processor and sent to the driver LSIs which in turn addresses the individual TFT cells.

Acting as an electro-optical switch, each TFT cell regulates light transmission from the backlight assembly when activated by the data source. By regulating the amount of light passing through the array of red, green, and blue dots, color images are created with clarity.

5. OUTLINE OF CHARACTERISTICS (at room temperature)

Display area	399.36(H) × 319.488(V)mm
Drive system	a-Si TFT active matrix
Display colors	Full-color
Number of pixels	1280 × 1024
Pixel arrangement	RGB vertical stripe
Pixel pitch	0.312(H) × 0.312(V)mm
Module size	470.0±0.5(H) × 382.0±0.5(V) × 45.0 typ.(D)mm
Weight	3460g(typ.)
Contrast ratio	220:1(typ.)
Viewing angle (more than the contrast ratio of 10:1)	Horizontal: 80° (typ. left side and right side) Vertical : 80° (typ. upper side and lower side)
Optimum grayscale	Perpendicular(γ=2.2)
Color gamut	40%(min., at center to NTSC)
Response time	58ms(typ.), "black" to "white"
Luminance	150cd/m^2(typ.)
Signal system	Analog RGB signals, Synchronous signals(Hsync, Vsync), CLK
Supply voltage	12V (Logic and LCD driving), 12V (Backlight)
Backlight	Ten cold cathode fluorescent lamps with an inverter
Power consumption	51.6W(typ.)

6. BLOCK DIAGRAM



note 1: FG(Frame ground) is connected to both GND and GNDB.

7. SPECIFICATIONS

7.1 GENERAL SPECIFICATIONS

Item	Specifications	Unit
Module size	470.0±0.5 (H) × 382.0±0.5 (V) × 48.0 max.(D)	mm
Display area	399.36 (H) × 319.488 (V)	mm
Number of pixels	1280 (H) × 1024 (V)	pixel
Dot pitch	0.104 (H) × 0.312 (V)	mm
Pixel pitch	0.312 (H) × 0.312 (V)	mm
Pixel arrangement	RGB (Red,Green,Blue) vertical stripe	-
Display colors	Full-color	color
Weight	3500 (max.)	g

7.2 ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit	Remarks
Supply voltage	VDD	-0.3 to +14	V	Ta = 25℃
	VDDB	0.0 to +14	V	
Logic input voltage	VIN1	-0.3 to +5.5	V	
R,G,B input voltage	VIN2	-6.0 to +6.0	V	
CLK input voltage	VIN3	-7.0 to +7.0	V	
VBL and VDAREF input voltage	VIN4	0.0 to +6.9	V	
BIAS input voltage	VIN5	0.0 to +12.7	V	
BRTL and FADJ input voltage	VIN6	0.0 to +3.5	V	
Storage temp.	Tst	-20 to +60	℃	-
Operating temp.	Top	0 to +50	℃	Module surface *
Humidity (No condensation)		≦ 95% relative humidity		Ta≦40℃
		≦ 85% relative humidity		40℃<Ta≦50℃
		Absolute humidity shall not exceed Ta=50℃, 85% relative humidity level.		Ta>50℃

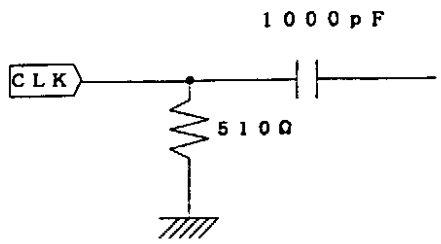
* Measured at the center of the LCD panel

7.3 ELECTRICAL CHARACTERISTICS
Logic/ LCD driving/ Backlight

Ta = 25℃

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage	VDD	11.4	12.0	12.6	V	for LCD driving
	VDDB	11.4	12.0	12.6	V	for backlight
Logic input "L" voltage	VIL	0	-	0.8	V	TTL level
Logic input "H" voltage	VIH	2.2	-	5.25	V	
CLK input voltage	VICLK	0.4	-	1.0	Vp-p	for CLK
CLK DC input level	VIdc-CLK	-4.5	-	+4.5	V	
Logic input "L" current 1	IIL1	-1.0	-	-	mA	for CNTSEL, CPSEL and POWC
Logic input "H" current 1	IIH1	-	-	10	μA	
Logic input "L" current 2	IIL2	-500	-	-	μA	for BRTC, ACA
Logic input "H" current 2	IIH2	-	-	300	μA	
Logic input "L" current 3	IIL4	-10	-	-	μA	for except above terminals
Logic input "H" current 3	IIH4	-	-	130	μA	
Video input voltage	VIRGB	0	-	0.7	Vp-p	for RGB Zi = 75Ω
Video input limits	VIdc-RGB	-3.5	-	+3.5	V	
Supply current (● dot-checkered pattern luminance maximum)	IDDB	-	3600	4900	mA	● VDDB=12V
	IDD	-	700	1100	mA	● VDD=12V

CLK input equivalent circuit



7.4 POWER SUPPLY SEQUENCE

(1) Logic signals (synchronous signals and control signals) should be "0" voltage (V), when VDD is not input. If higher than 0.3 V is input to signal lines, the internal circuit will be damaged.

(2) LCD module will shut down the power supply of driving voltage to LCD panel internally, when one of CLK, Hsync, Vsync, and DE(at DE mode) is not input more than 90 ms typically. During this period, the display data are unstable. But the backlight works correctly even this period, and the backlight can be controlled by BRTC signal.

(3) The ON/OFF switching of backlight while logic signals are supplied. The backlight power supply (VDDB) is not related to the power supply sequence. However, unstable data will be displayed when the backlight power is turned ON/OFF with no logic signals.

(4) Keep POWC signal "L" more than 200 ms after the power supply (VDD) is input, if POWC signal is controlled.

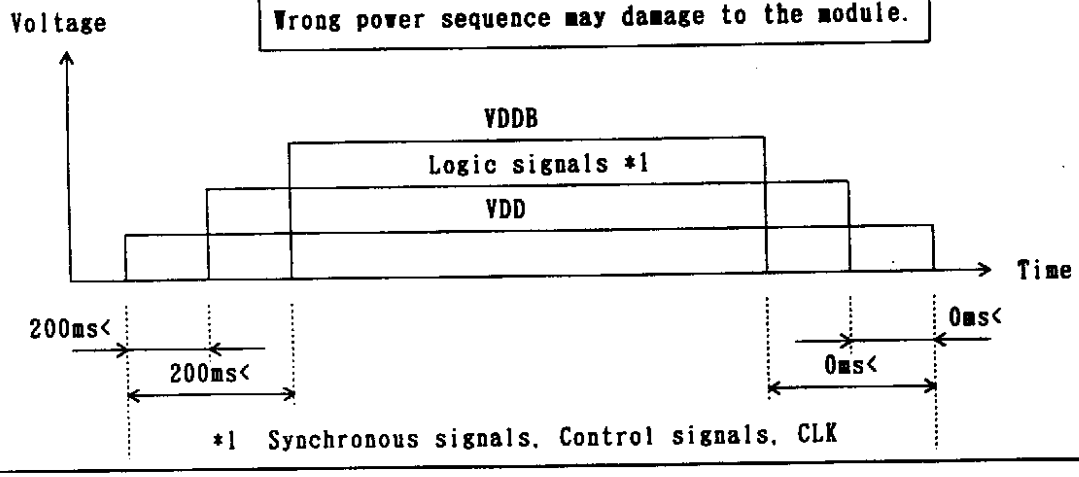
(5) Analog RGB inputs are independent from this power supply sequence.

(6) Ripple of supply voltage

	VDD (for logic and LCD driver)	VDDB (for backlight)
Acceptable range	≦ 100 mVp-p	≦ 200 mVp-p

note 1: The acceptable range of ripple voltage includes spike noises.

CAUTION
Wrong power sequence may damage to the module.



*1 Synchronous signals, Control signals, CLK

7.5 INTERFACE PIN CONNECTIONS

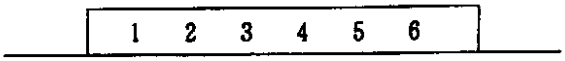
(1) CN 1

Part No. : MRF03-6R-SMT
Adaptable socket: MRF03-2×6P-1.27(For cable type) or
MRF03-6PR-SMT(For board to board type)
Supplier : HIROSE ELECTRIC CO.,LTD. (coaxial type)

Coaxial cable : UL20537PF75VLAS
Supplier : HITACHI CO., LTD.
note: A shield of coaxial cable should be connected with GND.

Pin No.	Symbol	Pin No.	Symbol
1	B	4	Vsync
2	G	5	Hsync
3	R	6	CLK

<Figure from socket view>



(2) CN 2

Part No. : IL-Z-12PL-SMTY
Adaptable socket: IL-Z-12S-S125C3
Supplier : Japan Aviation Electronics Industry Limited (JAE)

Pin No.	Symbol	Pin No.	Symbol
1	VDD	7	N.C.
2	VDD	8	N.C.
3	GND	9	DESEL
4	GND	10	GND
5	POWC	11	GND
6	GND	12	DE

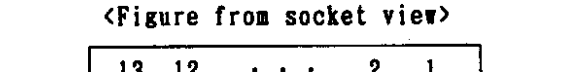
<Figure from socket view>

(3) CN 3

Part No. : IL-Z-13PL-SMTY
Adaptable socket: IL-Z-13S-S125C3
Supplier : Japan Aviation Electronics Industry Limited (JAE)

Pin No.	Symbol	Pin No.	Symbol
1	GND	8	CLAMP
2	CNTSEL	9	GND
3	CNTDAT	10	FIELD
4	CNTSTB	11	GND
5	GND	12	N.C.
6	CNTCLK	13	GND
7	CPSEL		

<Figure from socket view>



note: N.C.(No Connection) should be open.

(4) CN 201

Part No. : DF3-8P-2H
Adaptable socket: DF3-8S-2C
Supplier : HIROSE ELECTRIC CO.,LTD.

Pin No.	Symbol	Pin No.	Symbol
1	GNDB	5	VDDB
2	GNDB	6	VDDB
3	GNDB	7	VDDB
4	GNDB	8	VDDB

<Figure from socket view>

8 7 · · · 2 1

(5) CN 202

Part No. : IL-Z-9PL-SMTY
Adaptable socket: IL-Z-9S-S125C3
Supplier : Japan Aviation Electronics Industry Limited (JAE)

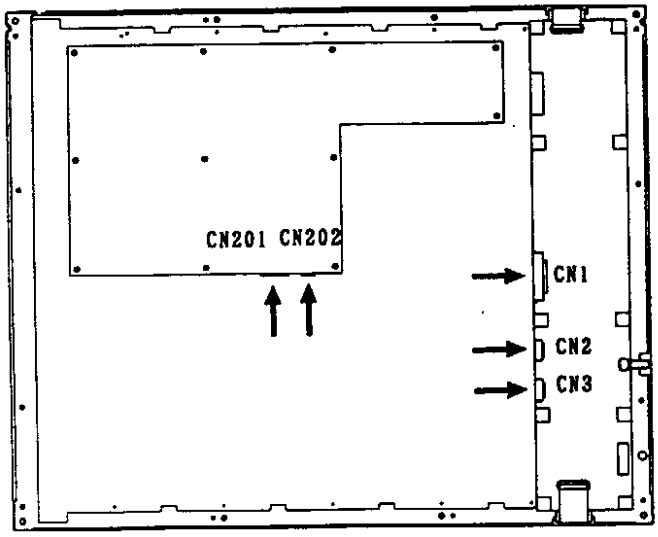
Pin No.	Symbol	Pin No.	Symbol
1	GNDB	6	BRTL
2	GNDB	7	N.C.
3	ACA	8	N.C.
4	BRTC	9	N.C.
5	BRTH		

note: N.C.(No Connection) should be open.

<Figure from socket view>

1 2 · · · 8 9

<Figure from socket view>



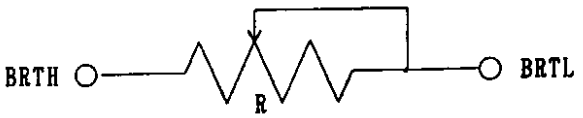
7.6 PIN FUNCTIONS

Symbol	Logic	I/O	Description
CLK	Positive	Input	Dot clock input. (ECL level) Timing signal for display data.
Hsync	Negative	Input	Horizontal synchronous signal input (TTL level)
Vsync	Negative	Input	Vertical synchronous signal input (TTL level)
DE	Positive	Input	Data enable signal input. (TTL level) Back-porch becomes free. When DESEL is "H". Back-porch becomes fix. When DESEL is "L". DE should be fixed "H" or "L". Don't use DE-FUNCTION when the display mode is SXGA-mode.
Red	–	Input	Red video signal input (0.7Vp-p, 75Ω)
Green	–	Input	Green video signal input (0.7Vp-p, 75Ω)
Blue	–	Input	Blue video signal input (0.7Vp-p, 75Ω)
CLAMP	–	Input	Clamp timing signal of black level (TTL level) Valid for only CPSEL is "L".
CNTSEL	–	Input	Display control signal in case of serial communication. (TTL level) {H or open: Default {L: External control
CNTDAT	Positive	Input	Display control data (serial data) (TTL level)
CNTCLK	Positive	Input	CLK for display control data (TTL level)
CNTSTB	Positive	Input	Latch pulse for display control data (TTL level)
DESEL	Positive	Input	DE function select signal (TTL level) {H: DE mode {L or open: Fixed mode
CPSEL	–	Input	Clamp signal function select signal (TTL level) {H or open: Default {L: CLAMP signal is possible
POWC	Positive	Input	Power control signal (TTL level) {H or open: Logic, LCD power is on {L: Logic, LCD power is off (*note 1)
BRTH BRTL	–	Input	Pins for backlight luminance control Variable resistor control (*note 2) or voltage control (*note 3)
BRTC	Positive	Input	Backlight ON/OFF control signal {H or open: Backlight on {L: Backlight off
ACA	Positive	Input	Luminance control signal {H or open: Normal luminance {L : Low luminance (1/2 of normal luminance)

Symbol	Logic	I/O	Description
VDD	–	Input	VDD (+12V±5%) power supply for LCD
VDDB	–	Input	VDDB (+12V±5%) power supply for backlight
GNDB	–	-	Ground for backlight (VDDB) GNDB is connected the module GND(FG).
GND	–	-	Signal ground for logic/LCD driving (VCC, VDD) (Connect to a system ground.)
FIELD	-	Field select signal(valid for only NTSC/PAL-mode) (TTL level) 1st field is "H" 2nd field is "L" Field terminal is possible to use "OPEN" in case of except NTSC/PAL-mode.	

note 1: When POWC is "L", logic input signal is all "0V". Please set the serial communication data, as the data are cleared. Also, if input is more than "0.3V", inside circuits of the LCD module may be broken.
When POWC is "L", serial communication data is clear, please set again.

note 2: The variable resistor for luminance control should be 10kΩ type, and zero point of the resistor correspond to the mimimum of luminance.



Mating variable resistor:
10KΩ±5% , B curve

Maximum luminance(100%): R= 10KΩ
Minimum luminance(30%: ACA="H", 60%: ACA="L"): R= 0Ω

note 3: If luminance is controlled by BRTH/BRTL input voltage, at first BRTH is "0V", and BRTL input voltage controls luminance. When BRTL input voltage is "1V", the luminance become maximum, and when BRTL input voltage is "0V", the luminance become minimum.
Maximum luminance(100%): BRTL="1V"
Minimum luminance(30%: ACA="H", 60%: ACA="L"): "0V"

7.7 FUNCTIONS

This LCD module has following functions by setting the serial data (table 1).

No.	FUNCTIONS	DETAIL
1	Expansion mode	See table.2 and 7.8 EXPANSION
2	Display position control (HORIZONTAL)	See table.6
3	Display position control (VERTICAL)	See table.3
4	CLK delay control	See table.4
5	Hsync period count number	See table.7
6	CLK fall/rise syncronus change	See table.6
7	Input frequency selection	See table.8

7.7.1 HOW TO USE THE ABOVE FUNCTIONS

If CNTSEL is "L", the above functions are valid. (CNTSEL is "H" or open, default values are valid.) After serial data are transferred, the data is latched by CNTSTB. Once, the data is latched, the above functions are effective.
Please keep CNTSTB at "L" during transferring data.

During setting the serial data when the power is switched on, the display may be unstable. NEC recommends that the backlight power is kept "off" by using BRTC function.

Table 1. CNTDAT COMPOSITION

Data	Data name	Function	Remarks
D0	VEX3	Expansion mode	See tabel 2
D1	VEX2	Expansion mode	
D2	VEX1	Expansion mode	
D3	VEX0	Expansion mode	
D4	VD10	Vertical display position (MSB)	See table 3
D5	VD9	Vertical display position	
D6	VD8	Vertical display position	
D7	VD7	Vertical display position	
D8	VD6	Vertical display position	
D9	VD5	Vertical display position	
D10	VD4	Vertical display position	
D11	VD3	Vertical display position	
D12	VD2	Vertical display position	
D13	VD1	Vertical display position	
D14	VD0	Vertical display position (LSB)	
D15	DELAY6	CLK delay (MSB)	See table 4
D16	DELAY5	CLK delay	
D17	DELAY4	CLK delay	
D18	DELAY3	CLK delay	
D19	DELAY2	CLK delay	
D20	DELAY1	CLK delay	
D21	DELAY0	CLK delay (LSB)	
D22	CKS	CLK reverse signal	See table 5
D23	HD8	Horizontal display position (MSB)	See table 6
D24	HD7	Horizontal display position	
D25	HD6	Horizontal display position	
D26	HD5	Horizontal display position	
D27	HD4	Horizontal display position	
D28	HD3	Horizontal display position	
D29	HD2	Horizontal display position	
D30	HD1	Horizontal display position	
D31	HD0	Horizontal display position (LSB)	
D32	HSE10	Horizontal count number (MSB)	See table 7
D33	HSE9	Horizontal count number	
D34	HSE8	Horizontal count number	
D35	HSE7	Horizontal count number	
D36	HSE6	Horizontal count number	
D37	HSE5	Horizontal count number	
D38	HSE4	Horizontal count number	
D39	HSE3	Horizontal count number	
D40	HSE2	Horizontal count number	
D41	HSE1	Horizontal count number	
D42	HSE0	Horizontal count number (LSB)	
D43	MOD1	CLK frequency select	See table 8
D44	MOD0	CLK frequency select	

Table 2. Display mode (VEX3 to VEX0: 4 bit)

VEX3	VEX2	VEX1	VEX0	Vertical magnification	Display mode	Display image
0	0	0	0	1	SXGA	Standard note 1
0	0	0	1	1.25	XGA	See display image
0	0	1	0	1.6	SVGA, MAC	
0	0	1	1	2.0	VGA	
0	1	0	0	2.5	PC98, VGA-TEXT	
0	1	0	1	-		
0	1	1	0	-	Prohibit	
0	1	1	1	4.0	NTSC	
1	0	0	X	-	Prohibit	
1	0	1	0	3.6	PAL	
1	0	1	1	-	Prohibit	
1	X	X	X	-	Prohibit	

note 1: Display mode is SXGA, when CNTSEL is "H" or "open".
note 2: VEX3 to VEX0 means D3 to D0 of CNTDAT.

Table 3. Vertical position (VD10 to VD0: 11 bit)

VD10	VD9	VD8	VD7	VD6	VD5	VD4	VD3	VD2	VD1	VD0	Vertical posi. [H]
0	0	0	0	0	0	0	0	0	0	0	Prohibit
0	0	0	0	0	0	0	0	0	0	1	Prohibit
0	0	0	0	0	0	0	0	0	1	0	Prohibit
0	0	0	0	0	0	0	0	0	1	1	Prohibit
0	0	0	0	0	0	0	0	1	0	0	4 note 1
0	0	0	0	0	0	0	0	1	0	1	5
.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	1	1	0	1	2045
1	1	1	1	1	1	1	1	1	1	0	2046
1	1	1	1	1	1	1	1	1	1	1	2047 Note 2

note 1: This is horizontal line number for effecting VIDEO signal from Vsync-fall.
note 2: The maximum vertical position is Vsync total.
note 3: Vertical position is fixed at 41H, when CNTSEL is "H" or "open".
note 4: VD10 to VD0 means D4 to D14 of CNTDAT.
note 5: When use DE-FUNCTION, display position can not be controlled.

Table 4. Clock(CLK) delay (DELAY6 to DELAY0: 7 bit)

DA(6:0)	Delay value
00H	7.0 ns
01H	7.6 ns
02H	8.2 ns
03H	8.8 ns
04H	9.4 ns
05H	10.0 ns
06H	10.5 ns
07H	11.2 ns
08H	11.8 ns
09H	12.4 ns
0AH	13.0 ns
0BH	13.7 ns
0CH	14.2 ns
0DH	14.8 ns
0EH	15.3 ns
0FH	15.9 ns
10H	16.6 ns
11H	17.2 ns
12H	17.8 ns
13H	18.4 ns
14H	18.9 ns
15H	19.5 ns
16H	20.1 ns
17H	20.7 ns
18H	21.4 ns
19H	22.0 ns
1AH	22.6 ns
1BH	23.2 ns
1CH	23.8 ns
1DH	24.4 ns
1EH	24.9 ns
1FH	25.6 ns
20H	26.3 ns
21H	26.9 ns
22H	27.4 ns
23H	28.1 ns
24H	28.5 ns
25H	29.1 ns
26H	29.7 ns
27H	30.3 ns
28H	31.0 ns
29H	31.6 ns
2AH	32.2 ns
2BH	32.8 ns

DA(6:0)	Delay value
2CH	33.3 ns
2DH	33.9 ns
2EH	34.4 ns
2FH	35.1 ns
30H	35.6 ns
31H	36.2 ns
32H	36.8 ns
33H	37.5 ns
34H	37.9 ns
35H	38.5 ns
36H	39.1 ns
37H	39.7 ns
38H	40.4 ns
39H	41.0 ns
3AH	41.5 ns
3BH	42.1 ns
3CH	42.6 ns
3DH	43.2 ns
3EH	43.8 ns
3FH	44.4 ns
40H	45.0 ns
41H	45.6 ns
42H	46.2 ns
43H	46.8 ns
44H	47.3 ns
45H	47.8 ns
46H	48.4 ns
47H	49.0 ns
48H	49.6 ns
49H	50.2 ns
4AH	50.8 ns
4BH	51.4 ns
4CH	51.9 ns
4DH	52.6 ns
4EH	53.1 ns
4FH	53.7 ns
50H	54.5 ns
51H	55.0 ns
52H	55.6 ns
53H	56.3 ns
54H	56.8 ns
55H	57.4 ns
56H	57.9 ns
57H	58.5 ns

DA(6:0)	Delay value
58H	59.2 ns
59H	59.8 ns
5AH	60.4 ns
5BH	61.1 ns
5CH	61.6 ns
5DH	62.2 ns
5EH	62.7 ns
5FH	63.3 ns
60H	64.0 ns
61H	64.7 ns
62H	65.3 ns
63H	66.0 ns
64H	66.5 ns
65H	67.1 ns
66H	67.7 ns
67H	68.3 ns
68H	68.9 ns
69H	69.5 ns
6AH	70.1 ns
6BH	70.7 ns
6CH	71.2 ns
6DH	71.9 ns
6EH	72.4 ns
6FH	73.1 ns
70H	73.6 ns
71H	74.2 ns
72H	74.8 ns
73H	75.4 ns
74H	75.9 ns
75H	76.5 ns
76H	77.0 ns
77H	77.7 ns
78H	78.3 ns
79H	79.0 ns
7AH	79.6 ns
7BH	80.2 ns
7CH	80.8 ns
7DH	81.4 ns
7EH	81.9 ns
7FH	82.5 ns

note 1: DA(6:0) means Delay 6(D15) to 0(D21 of CNTDAT.

<EXAMPLE>
DA(6:0)=00H

D15	16	17	18	19	20	21
0	0	0	0	0	0	0

DA(6:0)=2AH

D15	16	17	18	19	20	21
0	1	0	1	0	1	0

note 2: Delay value is approximate.

note 3: DA(6:0) is fixed at 00H. when CNTSEL is "H" or "open". This value is the upper limit by setting MOD as follow.

MOD1	MOD0	Upper limit of VD6 to VD0 CLK-delay setting (HEXADECIMAL)
0	0	49H
0	1	59H
1	0	6BH
1	1	7FH

note 4: This delay value is a typical value at Ta=25℃. And the value varies by the ambient temperature and the module itself.

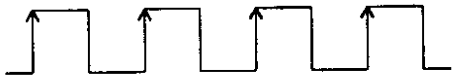
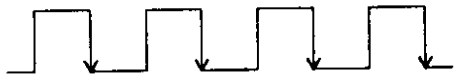
Please set up a preferable display position. See the following references.

① Variation of CLK delay by temperature drift. (only reference)
The temperature constant of CLK delay is 0.2 %/℃.

Calculated example:
In case of delay time is 20 ns at Ta=25℃:
(a) In case Ta rising to 50℃.
Increase of delay time → (50℃ − 25℃) × 0.002 × 20 ns = +1ns
So, the total delay time is 21 ns at Ta=50℃.
(b) In case Ta falling to 0℃.
Decrease of delay time → (0℃ − 25℃) × 0.002 × 20 ns = -1ns
So, the total delay time is 19 ns at Ta=0℃.

② Variation of CLK delay time. (as reference)
-10.5 % to +14.4 %

Table 5. CLK reverse signal

CKS	FUNCTION
0	Data is sampled on rising edge of CLK. 
1	Data is sampled on falling edge of CLK. 

note 1: CKS is "0", when CNTSEL is "H" or "open".
note 2: CKS means D22 of CNTDAT.

Table 6. Display horizontal position (HD8 to HD0: 9 bit)

HD8	HD7	HD6	HD5	HD4	HD3	HD2	HD1	HD0	Horizontal position [CLK]	
0	0	0	0	0	0	0	0	0	Prohibit	
0	0	0	0	0	0	0	0	1	Prohibit	
·	·	·	·	·	·	·	·	·	·	
·	·	·	·	·	·	·	·	·	·	
0	0	0	1	1	1	1	1	1	Prohibit	
0	0	1	0	0	0	0	0	0	110	note 1
0	0	1	0	0	0	0	0	1	111	
·	·	·	·	·	·	·	·	·	·	
·	·	·	·	·	·	·	·	·	·	
1	1	1	1	1	1	1	0	1	509	
1	1	1	1	1	1	1	1	0	510	
1	1	1	1	1	1	1	1	1	511	

note 1: This is the number of CLK between Hsync-fall and RGB data valid.
note 2: Horizontal position is set at 360 CLK, when CNTSET is "H" or "open".
note 3: HD8 to HD0 means D23 to D31 of CNTDAT.
note 4: When use DE-FUNCTION, display position can not be controlled.

Table 7. Display horizontal CLK numbers (HSE10 to HSE0: 11 bit)

HSE10	HSE9	HSE8	HSE7	HSE6	HSE5	HSE4	HSE3	HSE2	HSE1	HSE0	CLK number
0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	0	0	0	1	1	3
0	0	0	0	0	0	0	0	1	0	0	4
·	·	·	·	·	·	·	·	·	·	·	·
·	·	·	·	·	·	·	·	·	·	·	·
·	·	·	·	·	·	·	·	·	·	·	·
1	1	1	1	1	1	1	1	1	0	1	2045
1	1	1	1	1	1	1	1	1	1	0	2046
1	1	1	1	1	1	1	1	1	1	1	2047

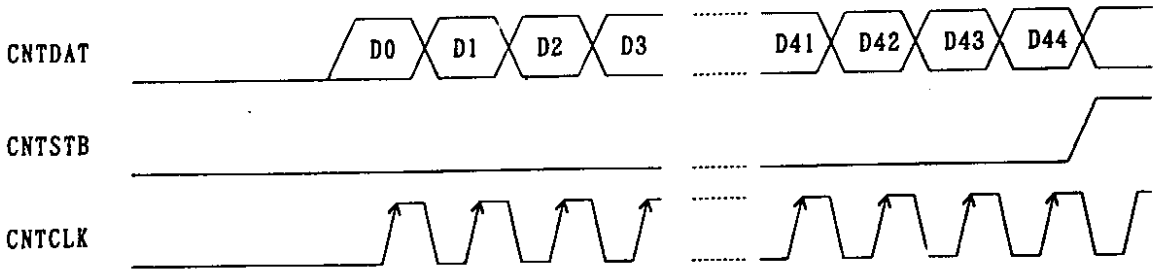
note 1: CLK number is from one falling edge of Hsync to the next Hsync.
note 2: CLK number is set 1688 CLK, when CNTSEL is "H" or "open".
note 3: This value sets CLK number of Hsync. If setting value is different from actual input signal, it cause to malfunction.
note 4: HSE10 to HSE0 means D32 to D42 of CNTDAT.

Table 8. Setting of CLK frequency (MOD1 to MOD0: 2 bit)

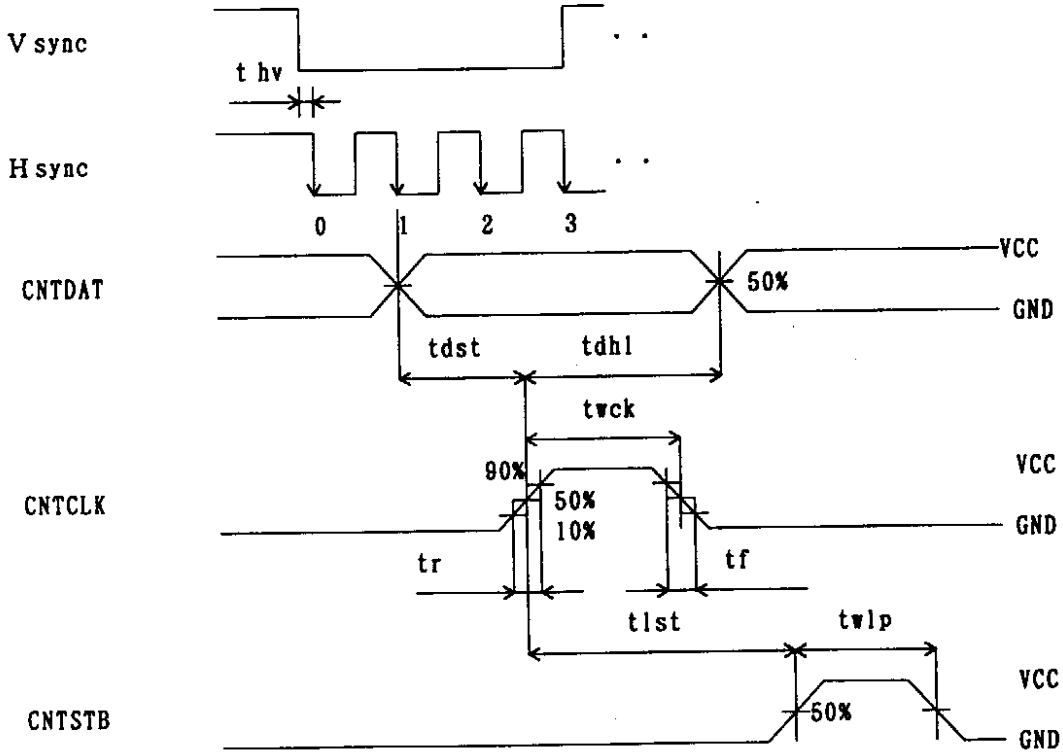
MOD1	MOD0	CLK frequency [MHz]
0	0	90 to 135
0	1	65 to 90
1	0	50 to 65
1	1	20 to 50

note 1: Set complying with input CLK frequency.
note 2: CLK frequency is set 90 to 135 MHz, when CNTSEL is "H" or "open".
note 3: MOD1 and MOD2 means D43 and D44 of CNTDAT.

7.7.2 SERIAL COMMUNICATION TIMINGS



Parameter	Symbol	Min.	Max.	Unit	Remarks
CLK pulse width	t wck	50	–	ns	CNTCLK
CLK frequency	f clk	–	5	MHz	
DATA setup-time	t dst	50	–	ns	CNTDAT
DATA hold-time	t dhl	50	–	ns	
Latch-pulse width	t wlp	50	–	ns	CNTSTB
Latch setup-time	t lst	50	–	ns	
Rise/fall time	tr, tf	–	50	ns	CNTxxx



7.8 EXPANSION

7.8.1 HOW TO USE EXPANSION MODES

Expansion mode is a function to expand screen. For example, SVGA signal has 800×600 pixels. But, if the display data can be expanded to 1.6 times vertically and horizontally, SVGA screen image can be displayed fully on the screen of SXGA resolution.

This LCD module has the function which expands vertical direction as shown in Table 1. And expanding horizontal direction is possible by setting input CLK frequency equivalent to the magnification. It is necessary to make this CLK outside of this LCD module.

The below image is display example, when DE function is default and HD and VD is set to most suitable frequency. And when DE function is used, HD and VD become default. Adjust the picture to the best position by DE signal.

Please adopt this mode after evaluating display quality, because the appearance in expansion mode is happened to be relatively bad in some cases.

The followings show display magnifications for each mode.

Input display	Resolution	Magnification	
		Vertical	Horizontal *
SXGA	1280 x 1024	1	1
XGA	1024 x 768	1.25	1.25
MAC	832 x 624	1.6	1.5
SVGA	800 x 600	1.6	1.6
VGA	640 x 480	2.0	2.0
VGA-TEXT	720 x 400	2.5	1.7
PC9801	640 x 400	2.5	2.0
PAL	Vertical 280 x 2	3.6	-
NTSC	vertical 240 x 2	4.0	-

* The horizontal magnification multiples the input clock(CLK).
  Input CLK = system CLK × horizontal magnification
  Example:
  In case of SXGA and SVGA, CLK frequency can be decided as follows.
  SXGA: System CLK(108.0MHz)×1.0=108.0MHz
  SVGA: System CLK(40.0MHz)×1.6= 64.0MHz

7.8.2 SETTING SERIAL DATA FOR EXPANSION

Input signal								Module serial-data setting		
Mode	System CLK [MHz]	H sync [KHz]	H sync [Hz]	Horizontal		Vertical		HSE	HD	VD
				Count number [CLK]	DSP* [CLK]	Count number [H]	DSP* [H]			
				(A)	(B)	—	(C)	Calculation formula		
								(A) × Hor. magni.	(B) × Hor. magni.	=(C)
SXGA										
VESA	108.0	63.981	60.02	1688	360	1066	41	(A) × 1	(B) × 1	=(C)
SUN	117.0	71.691	67.189	1632	336	1067	41			
EWS4800	125.0	75.120	71.204	1664	352	1055	28			
SGI	130.076	76.968	72.000	1690	378	1069	42			
HP	135.0	78.125	72.005	1728	384	1085	58			
VESA	135.0	79.976	75.025	1688	392	1066	41			
XGA								(A) × 1.25	(B) × 1.25	
VESA	65.000	48.363	60.004	1344	296	806	35			
VESA	75.000	56.476	70.069	1328	280	806	35			
VESA	78.750	60.023	75.029	1312	272	800	31			
MAC	57.283	49.725	74.55	1152	288	667	42	(A) × 1.5	(B) × 1.5	
SVGA								(A) × 1.6	(B) × 1.6	
VESA	36.000	35.156	56.25	1024	200	625	24			
VESA	40.000	37.879	60.317	1056	216	628	27			
VESA	50.000	48.077	72.188	1040	184	666	29			
VESA	49.500	46.875	75.000	1056	240	666	24			
VGA								(A) × 2.0	(B) × 2.0	
IBM	25.175	31.469	59.940	800	144	525	35			
VESA	31.500	37.861	72.809	832	168	520	31			
VESA	31.500	37.500	75.000	840	184	500	19			
MAC	30.24	35.0	66.667	864	160	525	42			
VGA-TEXT								(A) × 1.7	(B) × 1.7	
IBM	28.322	31.469	70.087	900	153	449	37			
PC9801	21.053	24.800	56.432	848	144	440	33	(A) × 2.0	(B) × 2.0	
PAL	25.000	15.625	50.000	-	256	312.5	9	1600	=(B)	
NTSC	25.197	15.734	59.94	-	256	262.5	9	1601	=(B)	

*: DSP=Display Start Period. DSP is total of "pulse-width" and "back-porch".

note 1: HD and VD are approximate value. Set HD and VD in case of adjusting display to the screen center.

note 2: The pulse-width of H sync, V sync and Back-porch are the same as SXGA-mode. (Standard-mode).

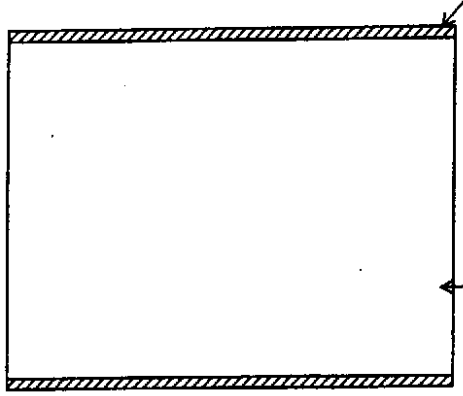
note 3: HSE see CLK number of table 7.

note 4: HD see horizontal position of table 6.

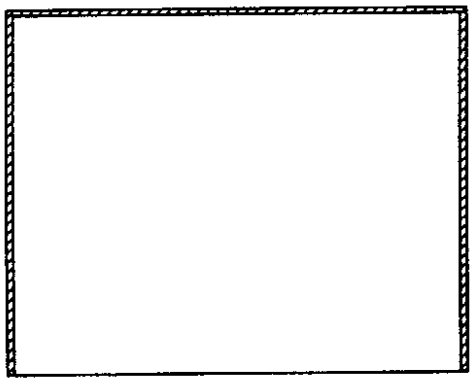
note 5: VD see vertical position of table 3.

7.8.3 DISPLAY IMAGES

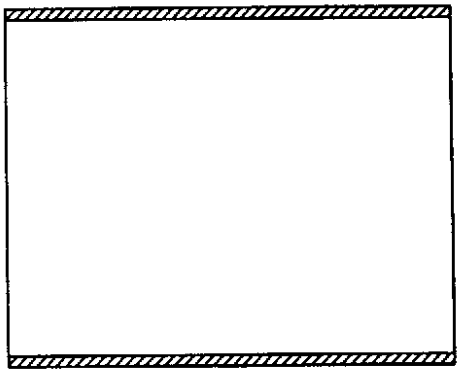
(1) XGA mode (1024×768)



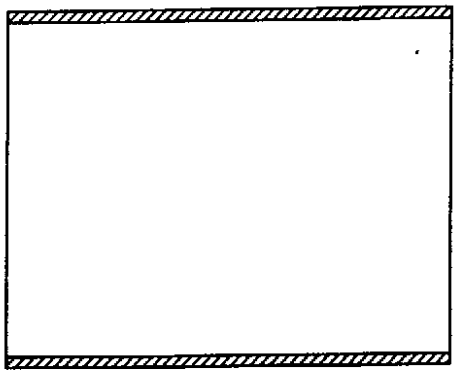
(2) MAC mode (832×624)



(3) SVGA mode (800×600)

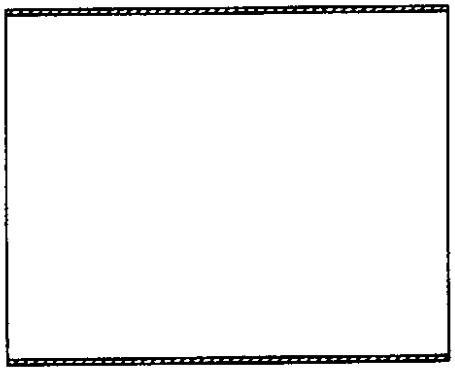


(4) VGA mode (640×480)



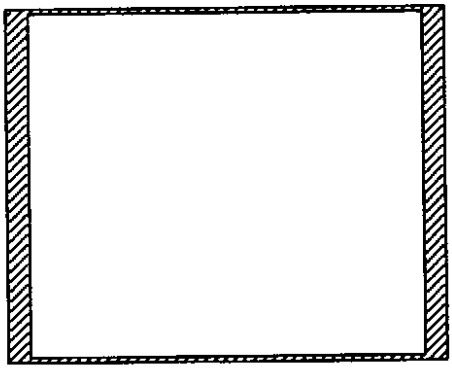
Horizontal: × 2.0 (1280 pixels)
Vertical : × 2.0 (960 pixels)

(5) PC9801 mode (640×400)



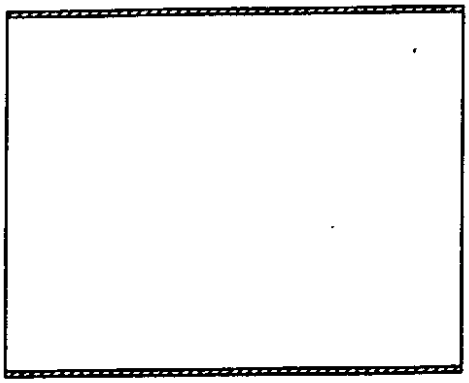
Horizontal: × 2.0 (1280 pixels)
Vertical : × 2.5 (1000 pixels)

(6) VGA-TEXT mode (720×400)



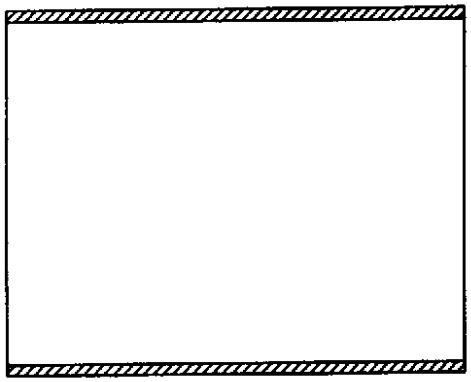
Horizontal: × 1.7 (1224 pixels)
Vertical : × 2.5 (1000 pixels)

(7) PAL mode (Vertical direction 280 ×2)



Vertical : × 3.6 (1008 pixels)

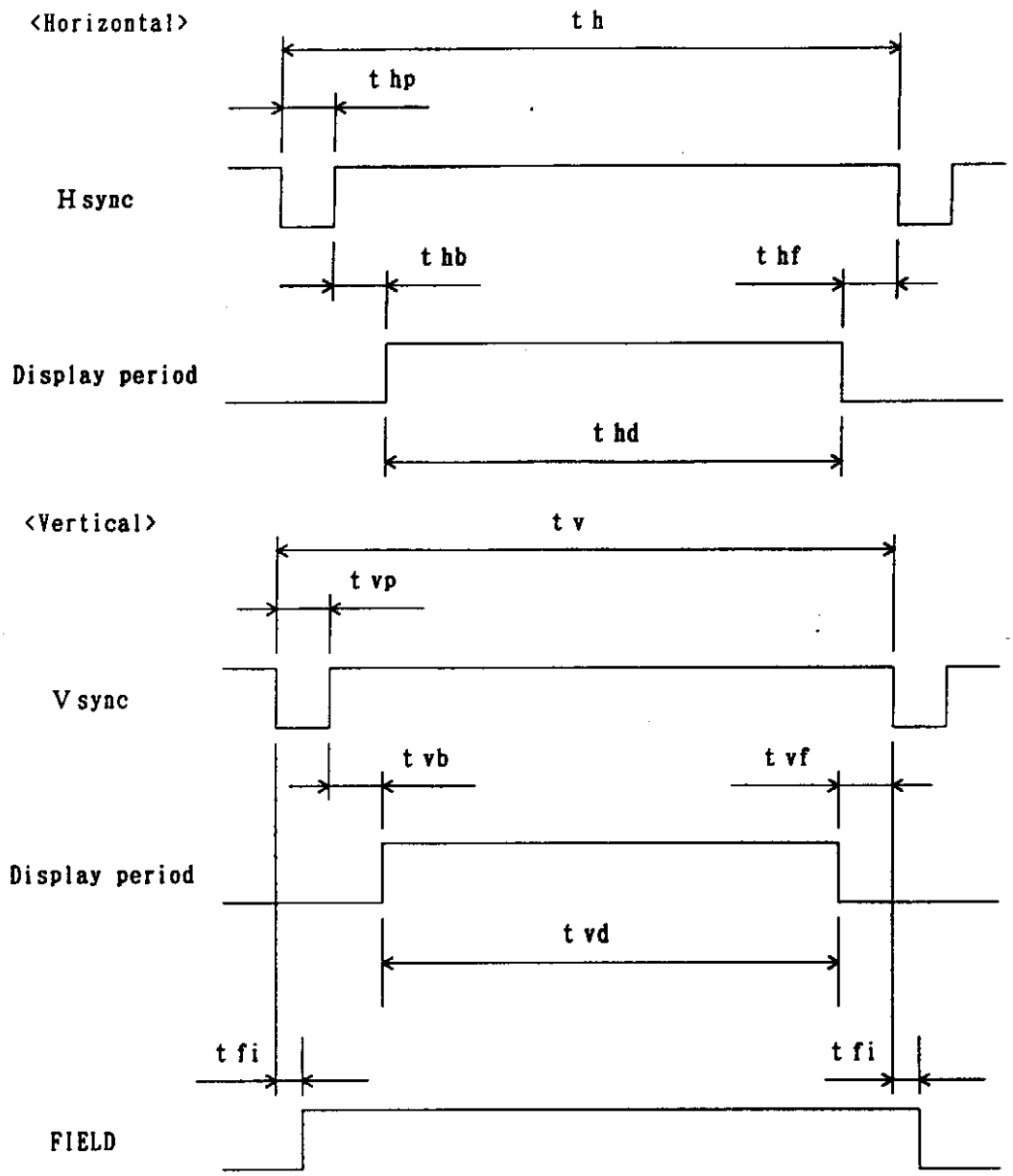
(8) NTSC mode (Vertical direction 240×2)

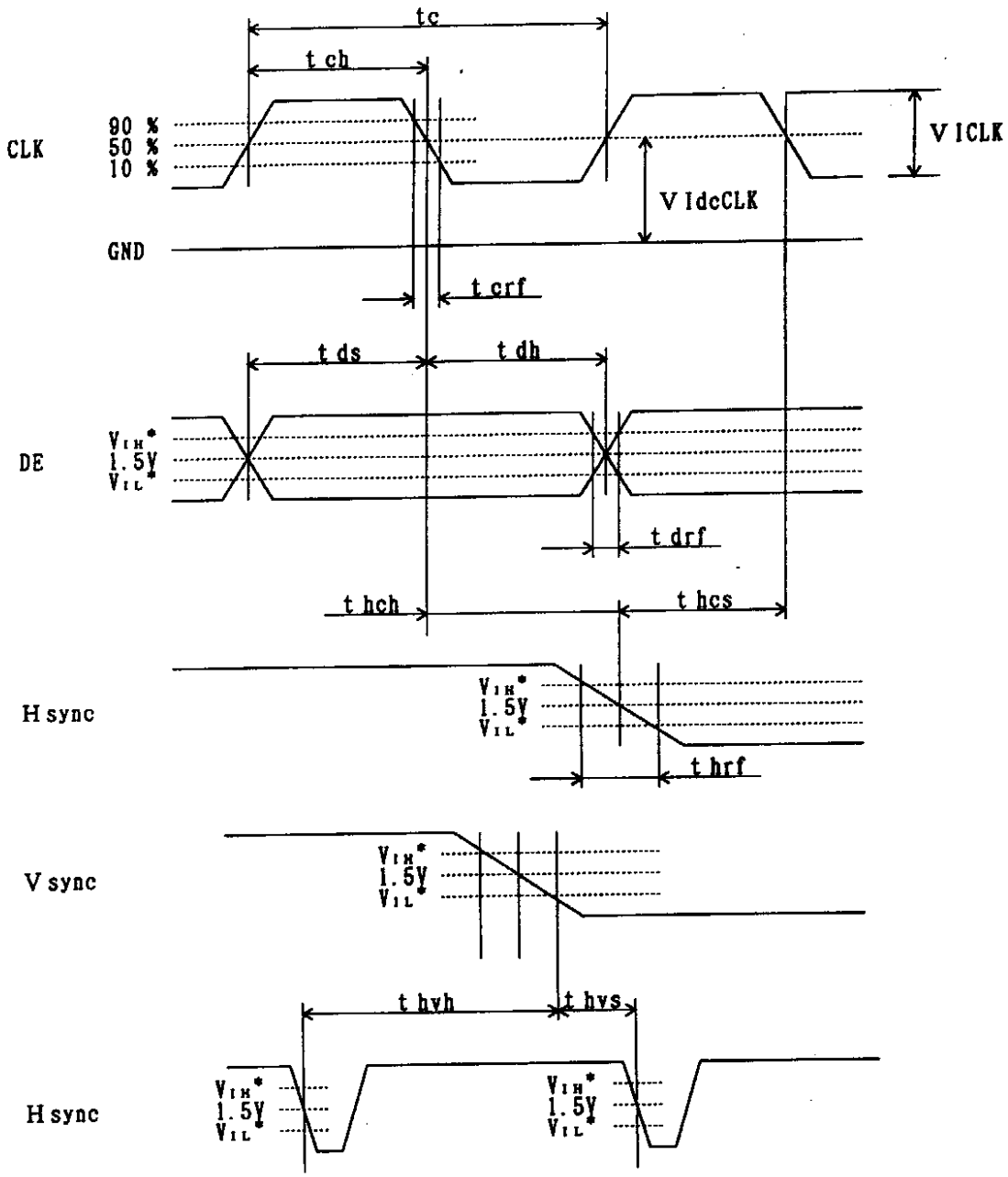


Vertical : × 4.0 (960 pixels)

7.9 INPUT SIGNAL TIMINGS
7.9.1 SXGA-MODE (Standard)

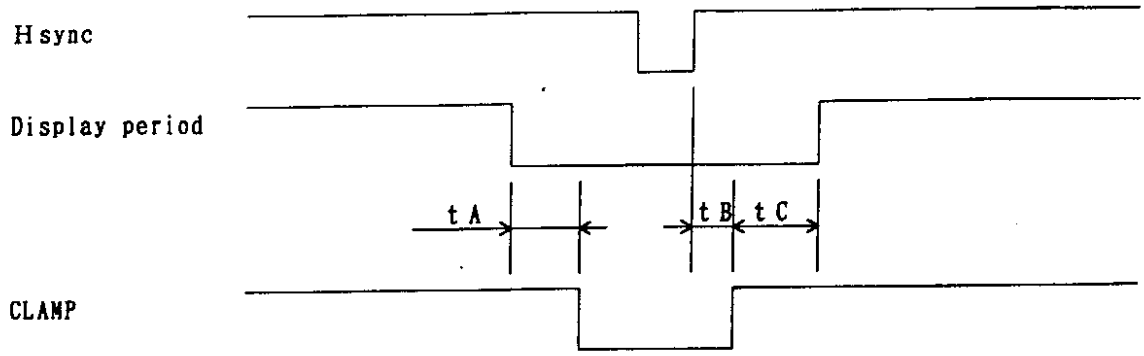
Name		Symbol	Min.	Typ.	Max.	Unit	Remarks
CLK	Frequency	1/t c	95.0 —	108.0 9.3	135.0 —	MHz ns	SXGA standard
	Rise/fall	t crf	—	—	10.0	ns	—
	Pulse-width	t ch /t c	0.4	0.5	0.6	—	—
Hsync	Period	t h	12.3 —	15.630 1688	17.0 —	μs CLK	63.981kHz (typ.)
	Display	t hd	— —	11.852 1280	— —	μs CLK	—
	Front-porch	t hf	— 10	0.444 48	— —	μs CLK	—
	Pulse-width	t hp	— 16	1.037 112	— —	μs CLK	—
	Back-porch	t hb	1.0 94	2.296 248	— —	μs CLK	—
	Pulse-width + Back-porch	t hpb	1.8	—	—	μs	—
	CLK-Hsync timing hold/setup time	t hch	4.0	—	—	ns	—
		t hcs	2.0	—	—	ns	—
	V-Hsync timing hold/setup time	t hvh	4.0	—	—	ns	—
		t hvs	1	—	—	CLK	
	Rise/fall	t hrf	—	—	10.0	ns	—
	Field timing	t fi	± 1	—	—	ns	—
Vsync	Period	t v	13.3 —	16.661 1066	18.5 —	ms H	60.020Hz (typ.)
	Display	t vd	— —	16.005 1024	— —	ms H	—
	Front-porch	t vf	— 1	0.016 1	— —	μs H	—
	Pulse-width	t vp	— 2	0.047 3	— —	μs H	—
	Back-porch	t vb	— 5	0.594 38	— —	μs H	—
DE	Setup time	t ds	2.0	—	—	ns	—
	Hold time	t dh	4.0	—	—	ns	—
	Rise/fall	t drf	—	—	10.0	ns	—
Analog R.G.B	Setup time	t das	2.0	—	—	ns	—
	Hold time	t dah	6.0	—	—	ns	—


<Horizontal>
t h
t hp
Hsync
t hb
t hf
Display period
t hd
<Vertical>
t v
t vp
Vsync
t vb
t vf
Display period
t vd
t fi
t fi
FIELD



* VIH= 2.2 V(MIN.)～VCC (MAX.)
VIL= 0 V(MIN.)～0.8 V(MAX.)

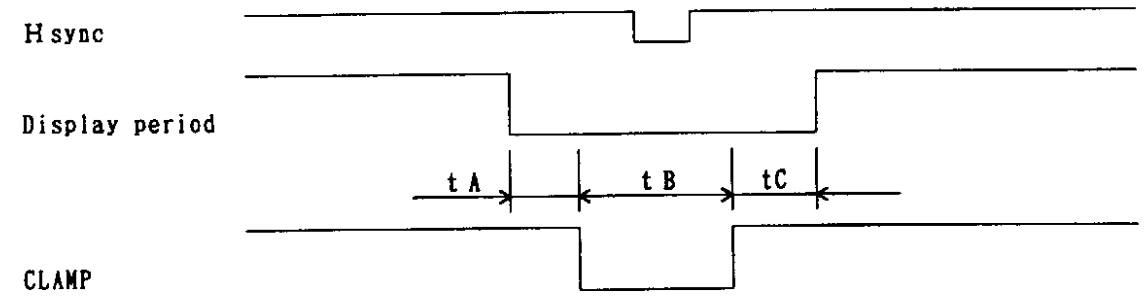
7.9.2 TIMING FOR GENERATING CLAMP SIGNAL INTERNALLY



MOD1	MOD0	tA[CLK]	tB[CLK]	tC[CLK]
0	0	62	46	200 minimum
0	1	44	32	
1	0	34	22	
1	1	28	18	

note 1: Exclude noises on analog R, G, B signal, because analog R, G, B signals are the black level reference during CLAMP="L". If noises are on the analog signals, luminance level of display is changed and the display becomes bad.

7.9.3 TIMING FOR INPUTTING CLAMP SIGNAL FROM OUTSIDE



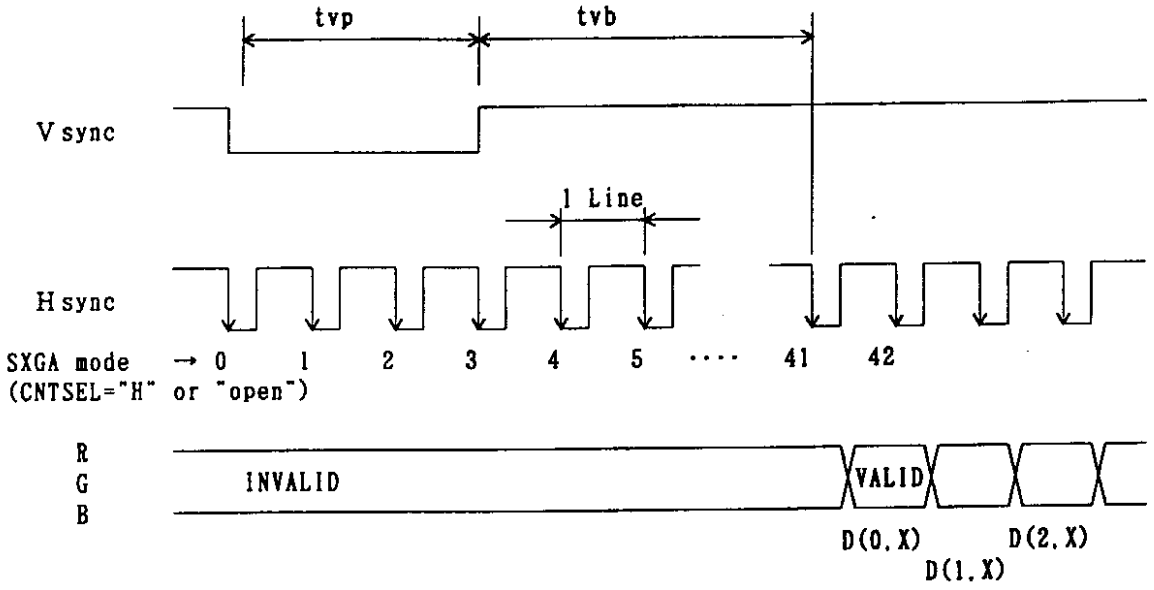
ITEMS	MIN.	TYP.	MAX.	Unit	Remarks
tA	0.1	–	–	μs	–
tB	0.3	–	–	μs	–
tC	0.2	–	–	μs	–

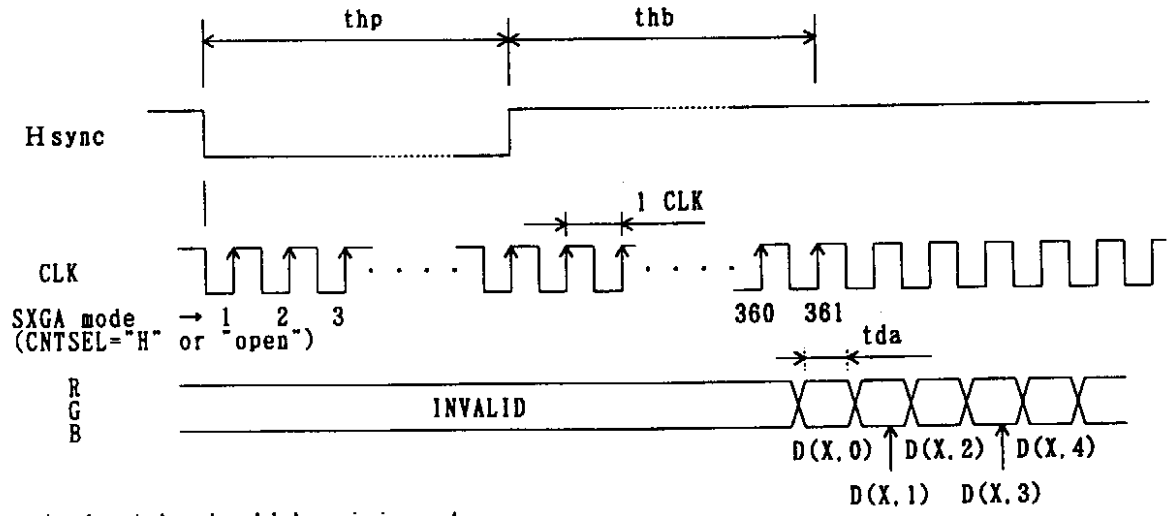
note 1: Exclude noises on analog R, G, B signal, because analog R, G, B signals are the black level reference during CLAMP="L". If noises are on the analog signals, luminance level of display is changed and the display becomes bad.

7.10 INPUT SIGNAL AND DISPLAY POSITION (SXGA STANDARD TIMING)
7.10.1 Fixed mode (DELSEL="L" or "Open")

Pixels

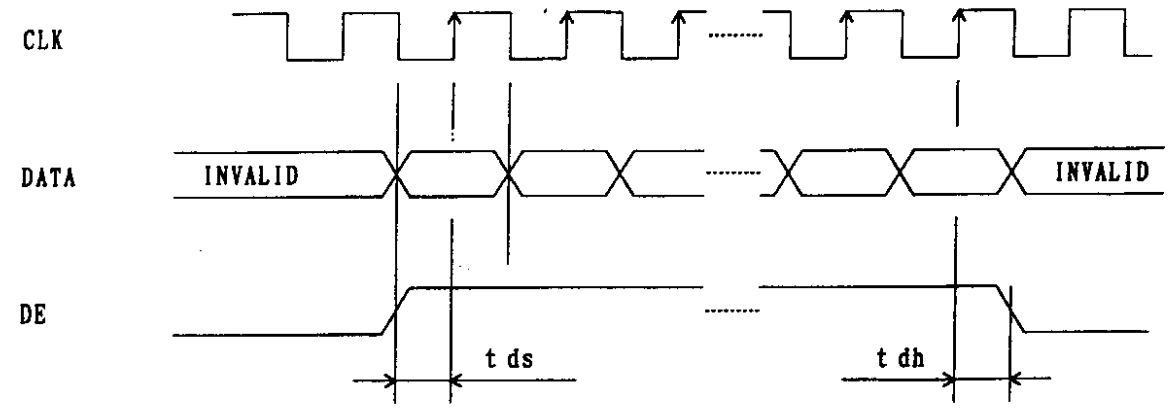
D(0, 0)	D(0, 1)	D(0, 2)	· · · · · ·	D(0,1279)
D(1, 0)	D(1, 1)			
D(2, 0)				
⋮				⋮
D(1023, 0)	D(1023, 1)	D(1023, 2)	· · · · · ·	D(1023,1279)

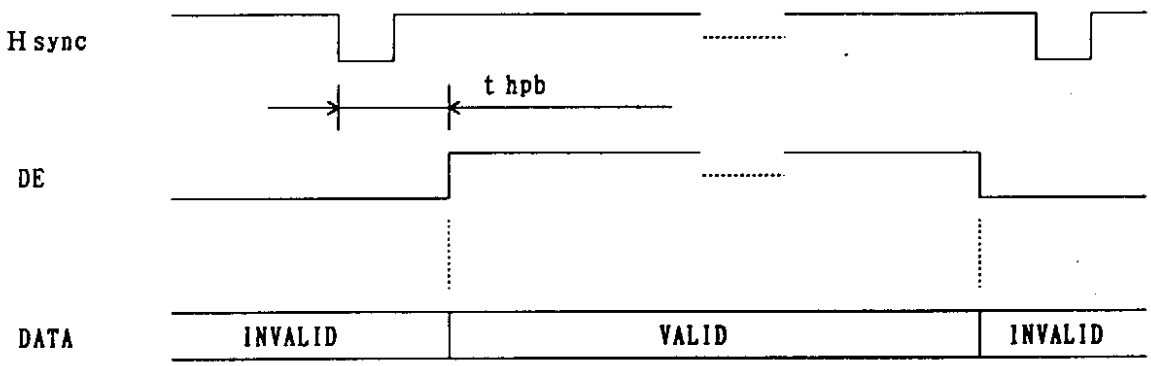


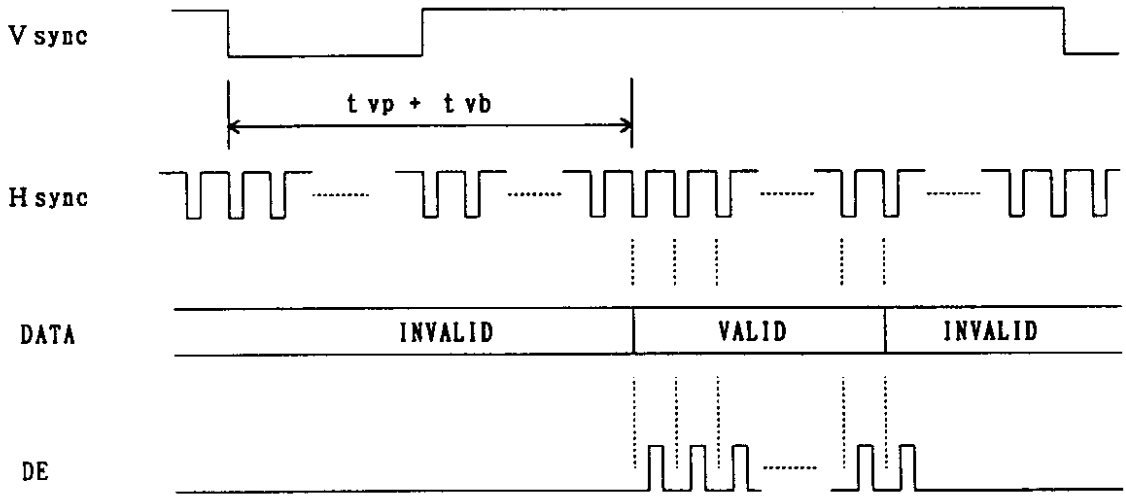


note 1: t da should be minimum 4ns.

7.10.2 DE mode (DELSEL="H")







7.11 OPTICAL CHARACTERISTICS

Ta = 25 ℃ note 1

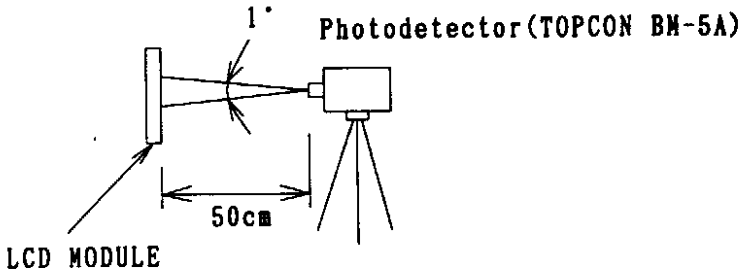
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Luminance	Lu	note 2	100	150	—	cd/m²	note 3
Contrast ratio	CR	$\theta x = \pm 0°$, $\theta y = \pm 0°$	150	220	—	—	note 4
Response time	tpd	black to white	—	58	130	ms	note 5
Color gamut	C	at center, to NTSC	40	—	—	%	—
Luminance uniformity	—	max./min.	—	—	1.30	—	note 6

Reference data

Ta = 25 ℃ note 1

Parameter		Symbol	Condition		Min.	Typ.	Max.	Unit	Remark
Viewing angle range	Horizontal	$\theta x+$	CR>10, $\theta y = \pm 0°$		70	80	—	deg.	note 7
		$\theta x-$	CR>10, $\theta y = \pm 0°$		70	80	—	deg.	
	Vertical	$\theta y+$	CR>10, $\theta x = \pm 0°$		70	80	—	deg.	
		$\theta y-$	CR>10, $\theta x = \pm 0°$		60	80	—	deg.	
Luminance control range by BRTH and BRTL		Maximum luminance 100 %		ACA= H	30 to 100			%	-
				ACA= L	60 to 100				

note 1: VDD = 12V, VDDB = 12V
note 2: Viewing angle is $\theta x = \pm 0°$, $\theta y = \pm 0°$. At center.
note 3: The luminance is measured with all pixels in "white" after the module runs 20 minutes.

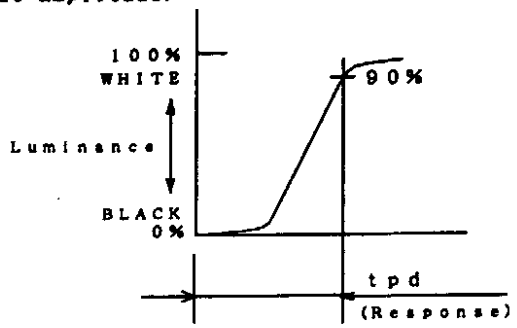


note 4: The contrast ratio is calculated by using the following formula.

$$\text{Contrast ratio(CR)} = \frac{\text{Luminance with all pixels in "white"}}{\text{Luminance with all pixels in "black"}}$$

The Luminance is measured in darkroom.

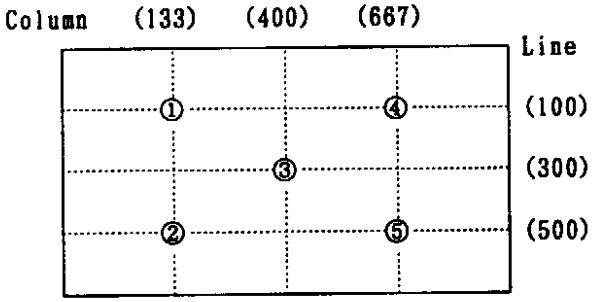
note 5: Definition of response time is as follows.
Photodetector output signal is measured when the luminance changes "black" to "white". Response time is the time between 0% and 90% of the photodetector output amplitude.



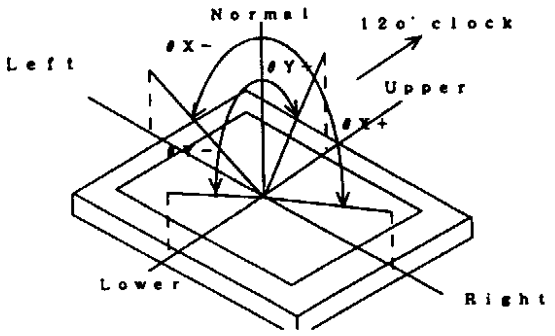
note 6: The luminance uniformity is calculated by using following formula.

$$\text{Luminance uniformity} = \frac{\text{Maximum Luminance}}{\text{Minimum Luminance}}$$

The luminance is measured at near the five points shown below.



note 7: Definitions of viewing angle are as follows.



8. GENERAL CAUTIONS

Next figures and sentence are very important, please understand these contents as follows.

⚠ CAUTION	This figure is a mark that you will get hurt and/or the module will have damages when you make a mistake to operate.
⚡	This figure is a mark that you will get an electric shock when you make a mistake to operate.
✋	This figure is a mark that you will get hurt when you make a mistake to operate

⚠ CAUTION

⚡	Do not touch an inverter --on which is stuck a caution label-- while the LCD module is under the operation, because of dangerous high voltage.

(1) Caution when taking out the module

① Pick the pouch only, in taking out module from a carrier box.

(2) Cautions for handling the module

① As the electrostatic discharges may break the LCD module, handle the LCD module with care against electrostatic discharges.

② ⚠ As the LCD panel and backlight element are made from fragile glass material, impulse and pressure to the LCD module should be avoided.

③ As the surface of polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.

④ Do not pull the interface connectors in or out while the LCD module is operating.

⑤ Put the module display side down on a flat horizontal plane.

⑥ Handle connectors and cables with care.

⑦ When the module is operating, do not lose CLK, Hsync, or Vsync signal. If any one of these signals is lost, the LCD panel would be damaged.

⑧ Don't put the front side(display surface side) of the module on a desk or a table for a long time, because the display may become un-uniformity.

(3) Cautions for the atmosphere

① Dew drop atmosphere should be avoided.

② Do not store and/or operate the LCD module in a high temperature and/or high humidity atmosphere. Storage in an electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.

③ This module uses cold cathod fluorescent lamp. Therefore, The life time of lamp becomes short conspicuously at low temperature.

④ Do not operate the LCD module in a high magnetic field.

(4) Caution for the module characteristics

① Do not apply fixed pattern data signal to the LCD module at product aging. Applying fixed pattern for a long time(more than 30 minutes) may cause image sticking.

(5)Other cautions

① Do not disassemble and/or reassemble LCD module.
② Do not readjust variable resistor or switch etc.
③ When returning the module for repair or etc. please pack the module not to be broken. We recommend to the original shipping packages.

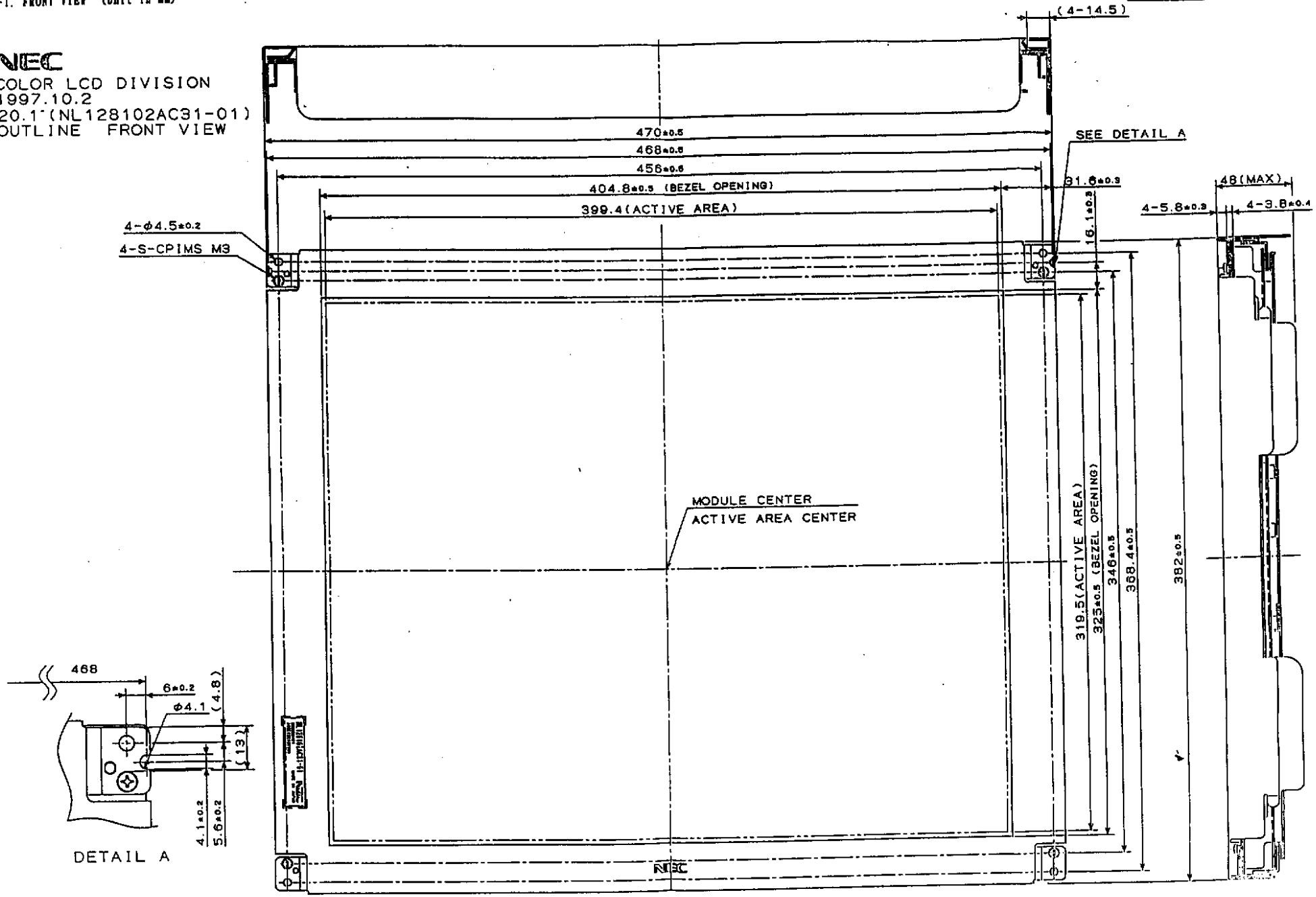
Liquid Crystal Display has the following specific characteristics. There are not defects or malfunctions.

The display condition of LCD module may be affected by the ambient temperature. The LCD module uses cold cathode tube for backlighting. Optical characteristics, like luminance or uniformity, will change during time.

Uneven brightness and/or small spots may be noticed depending on different display patterns.

9. OUTLINE DRAWING
9-1. FRONT VIEW (Unit in mm)

NEC
COLOR LCD DIVISION
1997.10.2
20.1"(NL128102AC31-01)
OUTLINE FRONT VIEW

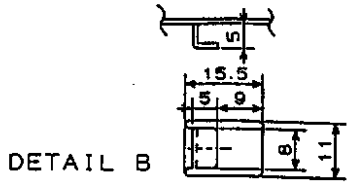


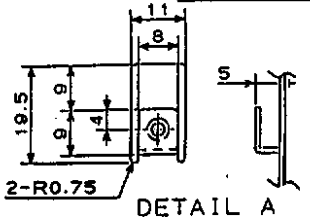
·THE VALUE IN PARENTHESE ARE FOR REFERENCE.

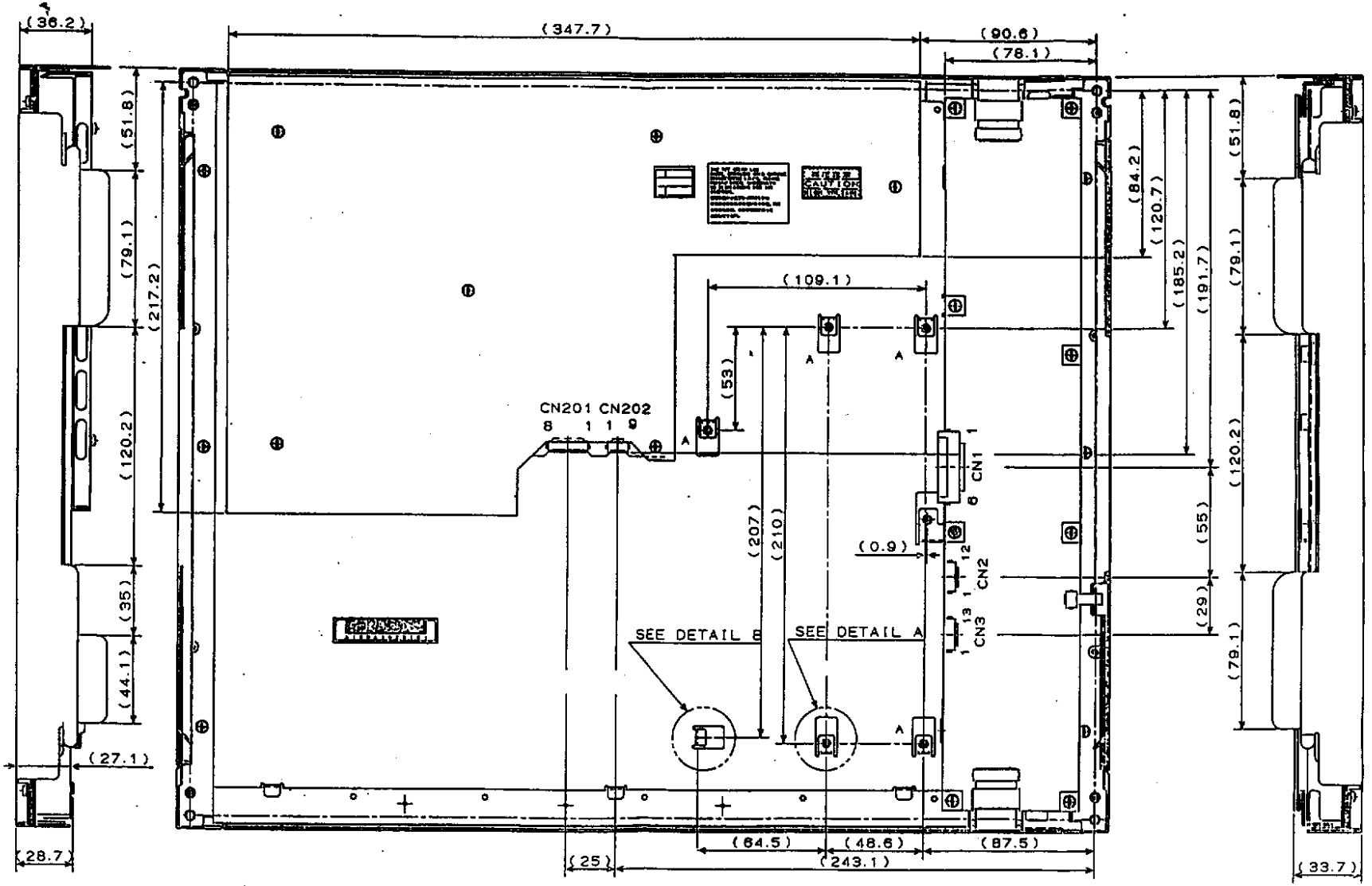
9-2. REAR VIEW (Unit in mm)

NEC

COLOR LCD DIVISION
1997.10.2
20.1"(NL128102AC31-01)
OUTLINE REAR VIEW







· THE VALUE IN PARENTHESE ARE FOR REFERENCE.

Rev.	Issued date	Revised contents	Approved	Checked	Prepared
1	Feb. 16, 1998	DOD-H-6024			