ITSV33N

30.8cm(12.1inch)SVGA(800x600) Color TFT LCD Module

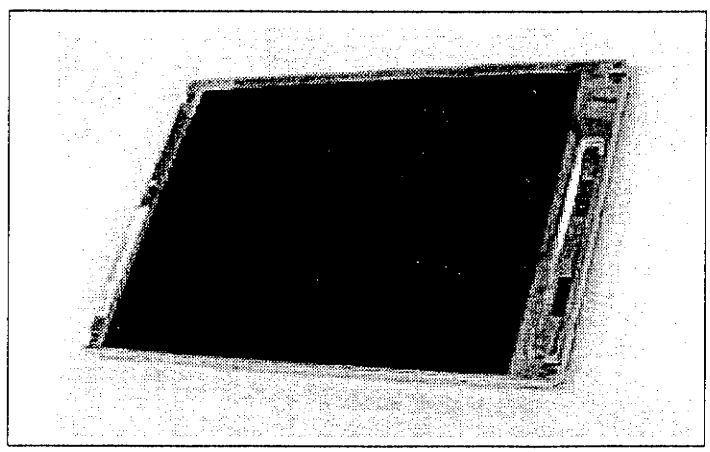
ITSV33N is a color TFT LCD module to be designed to realize the largest screen on A4 size notebook style personal computer. In addition to its large screen,the characteristics of this module are light weight, slim/thin outline, low power consumption and high resolution of SVGA(800x600) capability. This module also contains the inverter for backlight unit.

Features

- 30.8cm(12.1inch) diagonal
- Native 262k colors (R/G/B 6bit each)
- SVGA 800 x 600 pixels
- Low Reflection (CrOx Black Matrix)
- 293mm x 203mm x 12.4mm typ. (include inverter)
- 800 g typ.
- 4.2 W typ. (with inverter)

Applications

- Notebook PCs
- Green PCs
- Monitors



Characteristics Summary

Screen Diagonal	30.8cm(12.1")
Active Area	246.0mm(H) x 184.5mm(V)
Pixel Format	800(x3) x 600
Pixel Pitch	0.3075(per one triad) x 0.3075
Pixel Arrangement	R,G,B Vertical Stripe
Display Mode	Normally White
Typical White Luminance Battery Mode AC Adapter Mode	 70 (Brightness highest position) cd/m^2 110 (Brightness highest position) cd/m^2
Contrast Ratio	100 : 1 Typ.
Optical Rise Time/Fall Time	30 msec. Typ.
Nominal Input Voltage VDD(Vcc for LCD) V33(Vcc for G/A) VBL(Vcc for BL)	 +5V (min.4.75V, max. 5.25V) +3.3V (min.3.14V, max. 3.47V) +6.5V to +21.0V
Typical Power Consumption(watt) Battery Mode (8.4V Typ.,Brightness Min.) Battery Mode (8.4V Typ.,Brightness Max.) AC Adapter Mode (20.0V Typ.,Brightness Max.)	(VDD line + V33 line + VBL line) 1.6W Typ.(1.5W w/o Inverter) 4.2W Typ.(3.3W w/o Inverter) 5.7W Typ.(4.2W w/o Inverter)
Weight (grams with an inverter)	800 Typ.
Physical size	293mm x 203mm x 12.4mm
Electrical Interface	Digital Video(6-bit for each color R/G/B) Sync. Signal (x4) Backlight Control (x2) Contrast Control (x2)
Support Color	Native 262k colors
Temperature Range Operating Storage	 +5 to +50 degC -20 to +60 degC

Absolute Maximum Ratings

Rating	Symbol	Value	Unit	Conditions
Supply Voltage	VDD V33 Vcfl	-0.3 to +7.0 -0.3 to +6.0 1300	V V Vrms	 Lamp Ignition Voltage
Lamp Current	Icfl	7	mArms	
Input Voltage	VINl	-0.3 to +5.25	V	
Storage Temperature	TST	-20 to + 60	degC	At the glass surface
Operation Temperature	TOP	0 to +50	degC	At the glass surface
Operation Humidity		5 to 80	%RH	Max wet bulb temp. 29 degC No condensation

Signal Interface

LCD DRIVE Connector		AMP	5-179369-0
Corresponding Connector		AMP	5-179373-0
Pin No.	Signal Name	Description	
18	+RED5	Red Data 5	(MSB)
19	+RED4	Red Data 4	
20	+RED3	Red Data 3	
22	+RED2	Red Data 2	
23	+RED1	Red Data 1	
24	+RED0	Red Data 0	(LSB)
		Red-Pixel-Data	Each red pixel's data consists of these 6 bits pixel data
10	+GREEN5	Green Data 5	(MSB)
11	+GREEN4	Green Data 4	
12	+GREEN3	Green Data 3	
14	+GREEN2	Green Data 2	
15	+GREEN1	Green Data 1	
16	+GREEN0	Green Data 0	(LSB)
		Gree-Pixel-Data	Each green pixel's data consists of these 6 bits pixel data
2	+BLUE5	Blue Data 5	(MSB)
3	+BLUE4	Blue Data 4	
4	+BLUE3	Blue Data 3	
6	+BLUE2	Blue Data 2	
7	+BLUE1	Blue Data 1	
8	+BLUE0	Blue Data 0	(LSB)
			Each blue pixel's data consists of these 6 bits pixel data
36	-DTCLK	Data Clock	The typical frequency is 40.000MHz.The signal is used to strobe the pixel data and +DSPTMG signals.All pixel data shall be valid at the falling edge when the +DSPTMG signal is high.

28	+DSPTMG	Display Timing	This signal strobed at the falling edge of -DTCLK.When the signal is high,the pixel data shall be valid to be displayed.
27	VSYNC	Vertical Sync	The signal is synchronized to -DTCLK.
26	HSYNC	Horizontal Sync	The signal is synchronized to -DTCLK.
38	CONT1	Contrast 1	Bottom voltage of external-VR for contrast control.This signal is connected to ground in the module.
39	CONT2	Contrast 2	Reference voltage of external-VR for contrast control.
40	CONT3	Contrast 3	Top voltage of external-VR for contrast control
29,30	VDD	+5V	
33,34	V33	+3.3V	
1,5,9,13,17,21,25, 31,32,35,37	GND	Signal Ground	
42,44		Reserved	Not allowed to connect any other signal
41,43,45,46,47,48 49,50		N.C.	No connection

Note: Output signals from system shall be Hi-Z state when VDD is off.

Signal Interface for Inverter

Inverter Connector		AMP	1-179369-6
Corresponding Connector		AMP	1-179373-6
Pin No.	Signal Name	Description	
9	+BL-ON	Backlight ON	The signal is not synchronized to -DTCLK. When the signal is high,backlight is active.This signal is used to control the backlight only.
11	+Bright	Backlight Bright	The signal is not synchronized to -DTCLK. When the signal is low, the brightness shall be low to reduce power consumption. This signal is effective for battery operation.
1,2,3,4	VBL	+8.4V(Battery) / +20V(AC Adapter)	
5,6,7,8	VBL-RTN	VBL Return(0V)	
13	GND	Signal Ground	
15	VDD	+5V	
10,12,14,16		Reserved	No connection

Signal Specification

R/G/B,DTCLK,DSPTMG,H/VSYNC signal specification				
Parameter	**Condition**	**Min.**	**Max.**	**Unit**
Vih	High level input voltage	2.0	5.0	V
Vil	Low level input voltage	0	0.8	V
Iih	High level input current	–	1.0	uA
Iil	Low level input current	–	-1.0	uA

Supported Video Timing Guide Line

	800x600/56Hz	800x600/60Hz	Unit
Dot Clock	36	40	MHz
Frame Rate	56.25	60.317	Hz
H-Freq.	35.156	37.879	kHz
Hsync Pol.	Both	Positive	
Vsync Pol.	Both	Positive	
H-Total	28.444 (1024)	26.400 (1056)	usec (dots)
H-Backporch	3.556 (128)	2.200 (88)	usec (dots)
H-Frontporch	0.667 (24)	1.000 (40)	usec (dots)
Hsync Pulse	2.0 (72)	3.2 (128)	usec (dots)
H-Blank	6.222 (224)	6.400 (256)	usec (dots)
H-Active	22.222 (800)	20.000 (800)	usec (dots)
V-Total	17.788 (625)	16.579 (628)	msec (lines)
V-Backporch	0.626 (22)	0.607 (23)	msec (lines)
V-Frontporch	0.028 (1)	0.026 (1)	msec (lines)
Vsync Pulse	0.057 (2)	0.106 (4)	msec (lines)
V-Blank	0.771 (25)	0.739 (28)	msec (lines)
V-active	17.067 (600)	15.840 (600)	msec (lines)

Note: Please contact IBM if you need to use a Video Timing other than above.

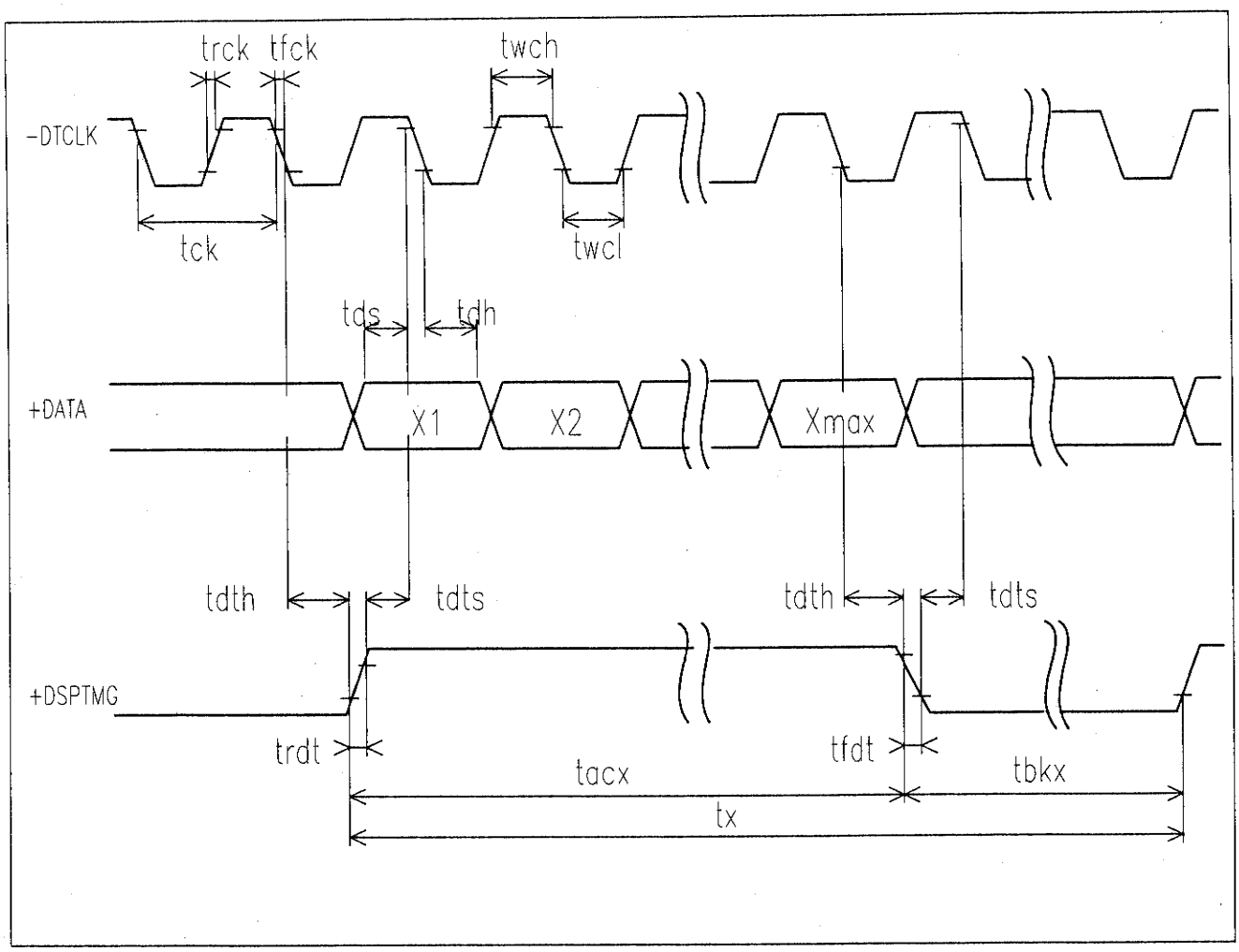
Interface Timing

Basically ,interface timings should match the VESA 800 x 600 60Hz manufacturing-guide line timing.

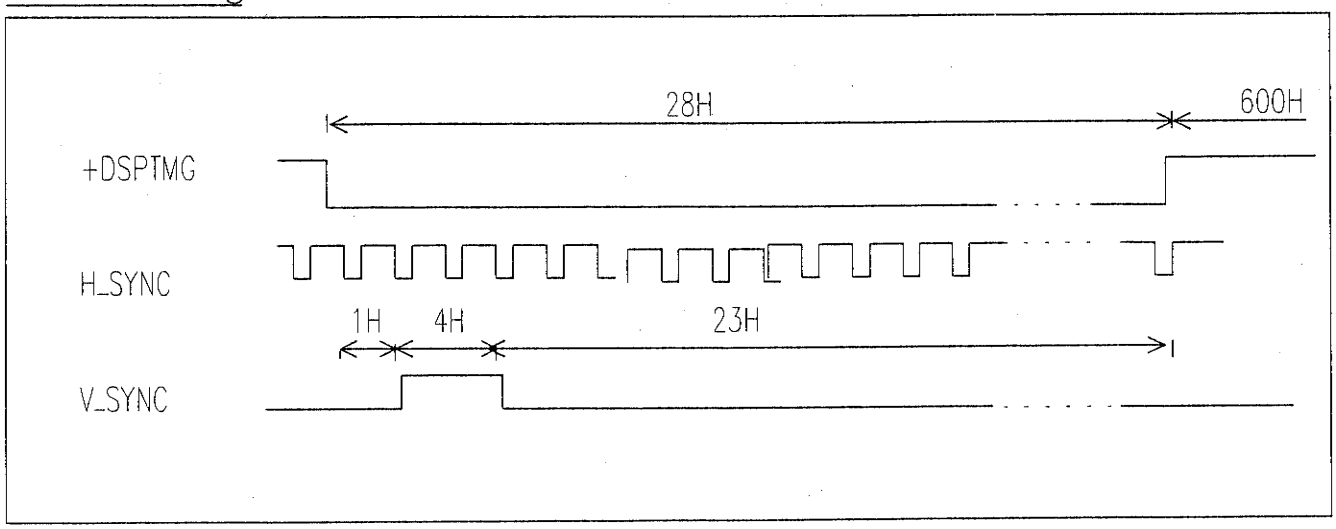
Symbol	Signal Description	MIN	TYP	MAX	UNIT
f_{dck}	DTCLK Frequency	35.82	40.00	40.20	MHz
t_{ck}	DTCLK cycle time	27.92	25.00	24.88	nsec
t_{wcl}	DTCLK low width	5.00			nsec
t_{wch}	DTCLK high width	5.00			nsec
t_{rck}	DTCLK rise time			3.00	nsec
t_{fck}	DTCLK fall time			3.00	nsec
t_{ds}	Data set up time	5.00			nsec
t_{dh}	Data hold time	5.00			nsec
t_{rdt}	DSPTMG rise time	5.00			nsec
t_{fdt}	DSPTMG fall time	5.00			nsec
t_{dts}	DSPTMG set up time	5.00			nsec
t_{dth}	DSPTMG hold time	5.00			nsec
t_x	X total time	1,000	1,056	1,080	t_{ck}
t_{acx}	X active time		800		t_{ck}
t_{bkx}	X blank time		256		t_{ck}
H_{sync}	H-frequency	35.16	37.88	38.46	KHz
t_y	Y total time	598	628	1,023	t_x
t_{acy}	Y active time	595	600		t_x
V_{sync}	Frame rate	56.00	60.00	61.00	Hz
V_w	V-sync width	2	4		t_x
V_{fp}	V-sync front porch	1	1		t_x
V_{bp}	V-sync back porch	10	23	31	t_x

Note: t_x (X total time) should be the same total time during 1 frame.

Horizontal Timing



Vertical Timing

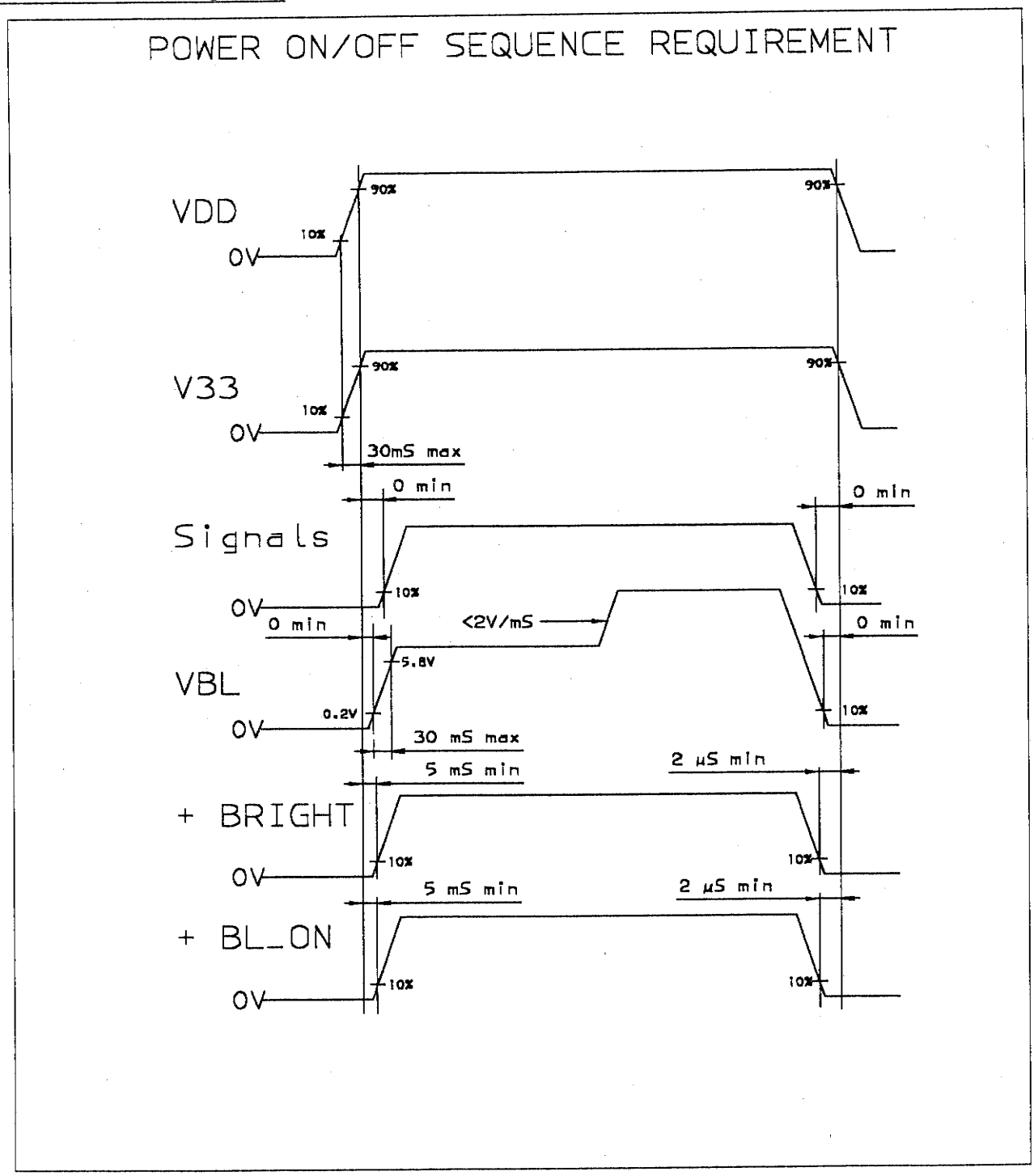


Power Requirement

SYMBOL	PARAMETER	Min.	Typ.	Max.	Unit	CONDITION
VDD	Logic/LCD Drive Voltage Backlight Logic Voltage	+4.75	+5.0	+5.25	V	
V33	Gate Array Drive Voltage	+3.14	+3.30	+3.47	V	
VBL(DC)	Backlight Voltage DC-mode	+6.5	+8.4	(+21.0)	V	
VBL(AC)	Backlight Voltage AC-mode	(+6.5)	+20.0	+21.0	V	
PDD	VDD Power		1.0	1.2	W	
P33	V33 Power		0.1	0.2	W	
PBL	VBL Power(w/inverter)		0.5 3.1 4.6	 3.6 5.5	W	DC-mode,Bright=L Min. Brightness DC-mode,Bright=L Max. Brightness AC-mode,Bright=H Max. Brightness
PDD+P33 +PBL	Total Power(w/inverter)		1.6 4.2 5.7	 5.0 6.9	W	DC-mode,Bright=L Min. Brightness DC-mode,Bright=L Max. Brightness AC-mode,Bright=H Max. Brightness (see Note:)
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			100	mVp-p	
VDDns	Allowable Logic/LCD Drive Ripple Noise			100	mVp-p	
V33rp	Allowable Gate Array Drive Ripple Voltage			100	mVp-p	
V33ns	Allowable Gate Array Drive Ripple Noise			100	mVp-p	
VBLrp	Allowable Backlight Ripple Voltage			100	mVp-p	
VBLns	Allowable Backlight Ripple Noise			250	mVp-p	

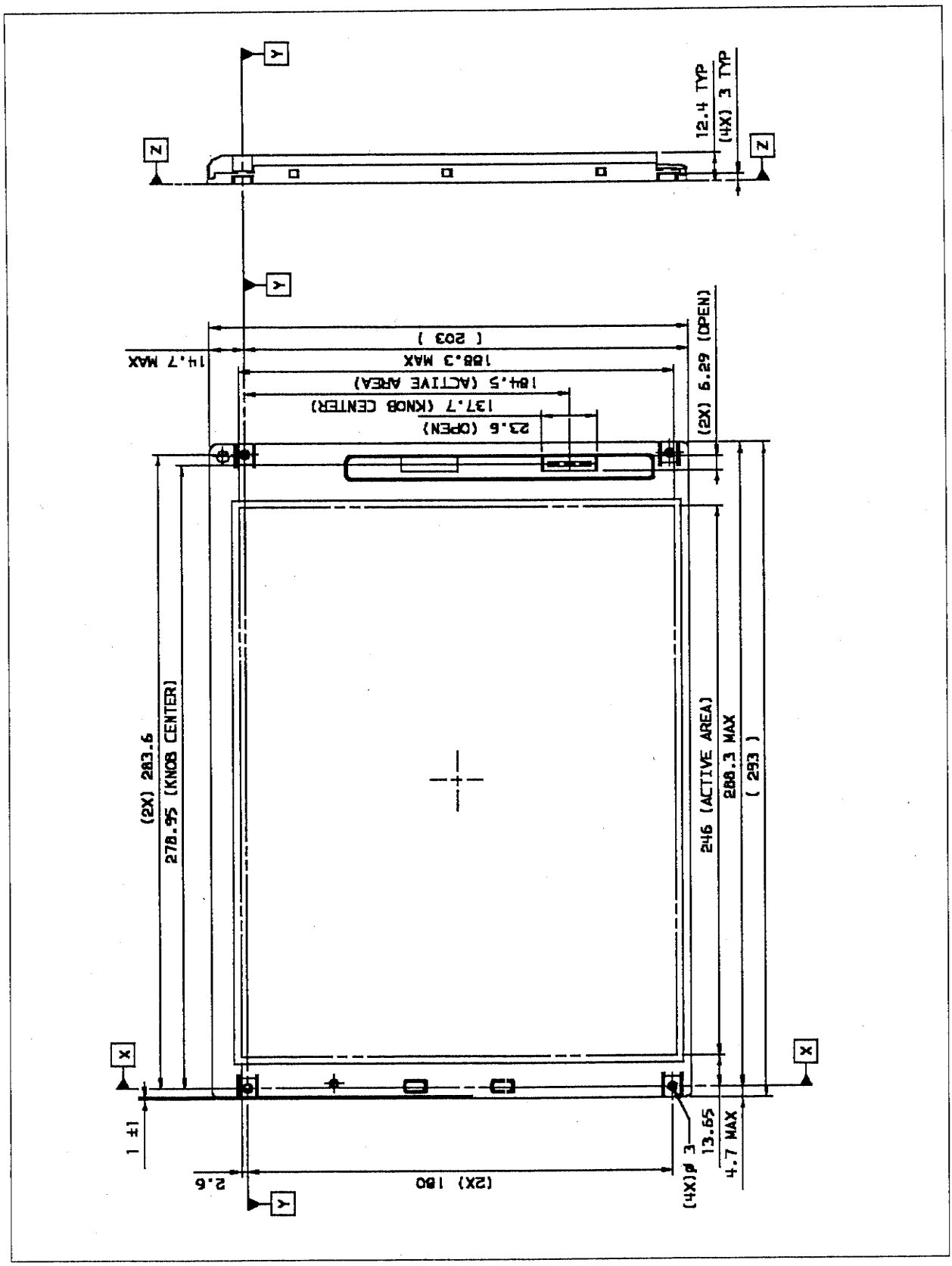
Note: These requirements shall be met with both 'All black pattern'.

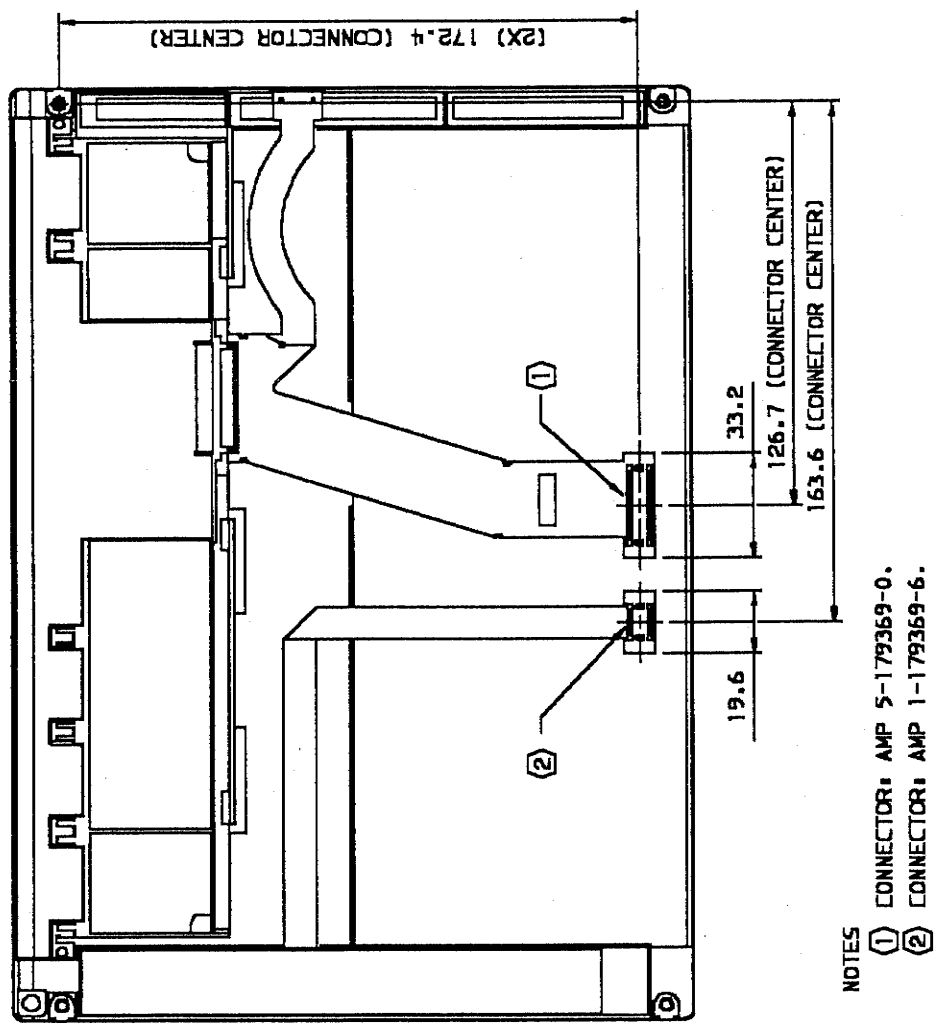
Power ON/OFF sequence



Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or creak if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.


12.4 TYP
(4X) 3 TYP
(203)
188.3 MAX
184.5 (ACTIVE AREA)
137.7 (KNOB CENTER)
23.6 (OPEN)
14.7 MAX
(2X) 6.29 (OPEN)
(2X) 203.6
278.95 (KNOB CENTER)
246 (ACTIVE AREA)
288.3 MAX
(293)
1 ±1
2.6
(2X) 180
(4X)ø 3
13.65
4.7 MAX


(2X) 172.4 (CONNECTOR CENTER)
33.2
126.7 (CONNECTOR CENTER)
163.6 (CONNECTOR CENTER)
19.6
NOTES
① CONNECTOR: AMP 5-179369-0.
② CONNECTOR: AMP 1-179369-6.