ITSV50E = 7349847

30.8cm(12.1 inch)SVGA(800x600) Color TFT LCD Module

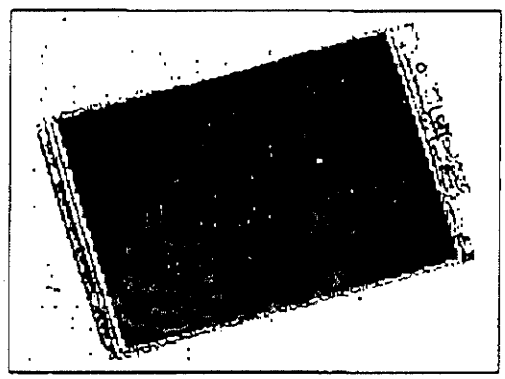
ITSV50E is a TFT LCD color module to be designed to realize the largest screen on A4 size notebook style personal computer. In addition to its large screen,the characteristics of this module are light weight, slim/thin outline, low power consumption and high resolution of SVGA(800x600) capability.

Features

- 30.8cm(12.1 inch) diagonal
- Native 262k colors (R/G/B 6bit each)
- SVGA 800 x 600 pixels
- Low Reflection (Black Matrix)
- 290mm x 200mm x 6.8mm typ. (with inverter)
- 470 g typ. (with inverter)
- 3.4 W typ.(with inverter)

Applications

- Notebook PCs
- Monitors



Preliminary

Characteristics Summary

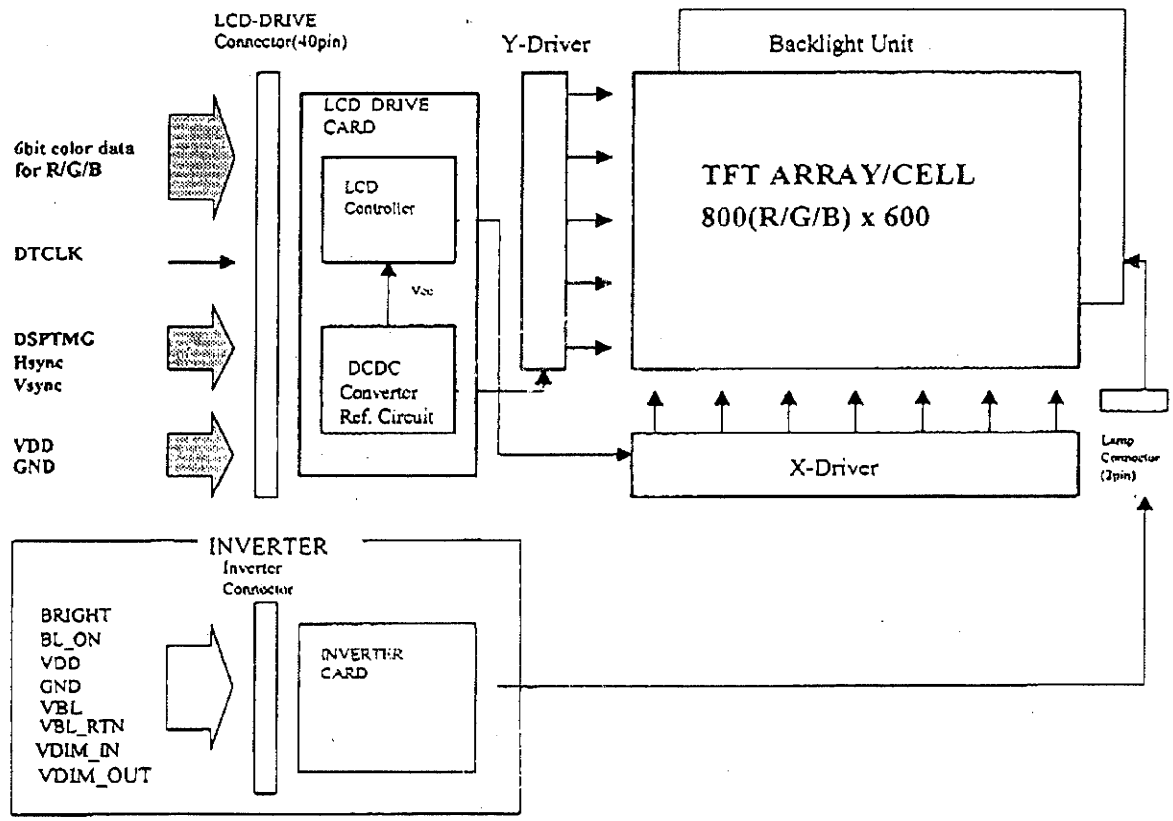
Screen Diagonal	30.8cm(12.1")
Active Area	246.0mm(H) x 184.5mm(V)
Pixel Format	800(x3) x 600
Pixel Pitch	0.3075(per one triad) x 0.3075
Pixel Arrangement	R,G,B Vertical Stripe
Display Mode	Normally White
Typical White Luminance Battery Mode AC Adapter Mode	 100 (Brightness highest) cd/m^2 160 (Brightness highest) cd/m^2
Contrast Ratio	100 : 1 Typ.
Optical Rise Time/Fall Time	30 msec. Typ.
Nominal Input Voltage VDD VBL	 +5V +6.5V to +21.0V (for inverter)
Typical Power Consumption Battery Mode AC Adapter Mode	(VDD line + VBL line) 3.4W Typ. 4.5W Typ.
Weight	470 grams Typ.
Physical Size	290mm x 200mm x 6.8mmTyp.
Electrical Interface	Digital Video(6-bit for each color R/G/B) Sync. Signal (x4) Backlight Control (x4 for inverter)
Supported Colors	Native 262k colors
Temperature Range Operating Storage	 +0 to +50 -20 to +60

Preliminary

Absolute Maximum Ratings

Rating	Symbol	Value	Unit	Conditions
Supply Voltage	VDD	-0.3 to +6.0	V	
	VBL	+23.0	V	
Input Signals of Inverter		VDD + 0.5	V	BL_ON/BRIGHT/VDIM_IN/ VDIM_OUT
Shock		50	G	18ms
Vibration		1.5	G	10-200Hz
Storage Temperature	TST	-20 to + 60	degC	At the glass surface
Operation Tempraute	TOP	0 to +50	degC	At the glass surface
Operation Humidity		8 to 95	%RH	Max wet bulb temp. 29 degC No condensation

Block Diagram



Signal Interface

LCD Drive Connector		AMP	4-179369-0
Corresponding Connector		AMP	4-179373-0
Pin No.	Signal Name	Description	
18	+RED5	Red Data 5	(MSB)
19	+RED4	Red Data 4	
20	+RED3	Red Data 3	
22	+RED2	Red Data 2	
23	+RED1	Red Data 1	
24	+RED0	Red Data 0	(LSB)
		Red-Pixel-Data	Each red pixel's data consists of these 6 bits pixel data
10	+GREEN5	Green Data 5	(MSB)
11	+GREEN4	Green Data 4	
12	+GREEN3	Green Data 3	
14	+GREEN2	Green Data 2	
15	+GREEN1	Green Data 1	
16	+GREEN0	Green Data 0	(LSB)
		Gree-Pixel-Data	Each green pixel's data consists of these 6 bits pixel data
2	+BLUE5	Blue Data 5	(MSB)
3	+BLUE4	Blue Data 4	
4	+BLUE3	Blue Data 3	
6	+BLUE2	Blue Data 2	
7	+BLUE1	Blue Data 1	
8	+BLUE0	Blue Data 0	(LSB)
			Each blue pixel's data consists of these 6 bits pixel data
36	-DTCLK	Data Clock	The typical frequency is 40.00MHz.This signal is used to strobe the pixel data and +DSPTMG signals.All pixel data shall be valid at the falling edge when the +DSPTMG signal is high.

28	+DSPTMG	Display Timing	This signal is strobed at the falling edge of -DTCLK.When the signal is high,the pixel data shall be valid to be displayed.
27	VSYNC	Vertical Sync	This signal is synchronized to -DTCLK.
26	HSYNC	Horizontal Sync	This signal is synchronized to -DTCLK.
29,30	VDD	+5V	
33,34		Reserved	
1,5,9,13,17,21,25, 31,32,35,37,40	GND	Signal Ground	
38		Reserved	No connection (Signal reserved)
39		Reserved	No connection (Signal reserved for contrast)

Note: Output signals from system shall be low or Hi-Z state when VDD is off.

Inverter Connector Signal Specification

LCD Drive Connector		AMP	1-179369-6
Corresponding Connector		AMP	1-179373-6
Pin No.	Signal Name	Description	
1, 2, 3, 4	VBL		Battery Mode +8.4 or +10.8V Typ. AC Mode +16.0 or +20.0V Typ.
5, 6, 7, 8	VBL_RTN	VBL return	0V
9	+ BL_ON	Backlight ON	This signal is not synchronized to -DTCLK. When the signal is high, Backlight is Active. This signal is used to control the Backlight only.
10, 12		Reserved	No connection (Signal Reserved)
11	+ BRIGHT	Backlight Bright	This signal is not synchronized to -DTCLK. When the signal is low, the brightness shall be low to reduce power consumption. This signal is effective for battery operation.
13	GND	Signal Ground	
14	VDIM_IN	Brightness Control Input	0V (Brightness Max.) to +4V (Brightness Min.). This signal shall be connected to VDIM_OUT at user side connector when the brightness potentiometer on the inverter card isused.
15	VDD	+5V	
16	VDIM_OUT	Brightness Control Output	

Note: Output signals from system shall be low or Hi-Z state when VDD is off.

Signal Specification

R/G/B,DTCLK,DSPTMG,H/VSYNC signal specification				
Parameter	**Condition**	**Min.**	**Max.**	**Unit**
Vih	High level input voltage	2.0	VDD +0.3	V
Vil	Low level input voltage	0	0.8	V
Iih	High level input current	–	50	uA
Iil	Low level input current	–	-50	uA
BL-ON, BRIGHT signal specification				
Vih	High level input voltage	3.5	VDD +0.3	V
Vil	Low level input voltage	0	0.7	V
Iih	High level input current	–	1.0	mA
Iil	Low level input current	–	-1.0	mA

Interface Timing

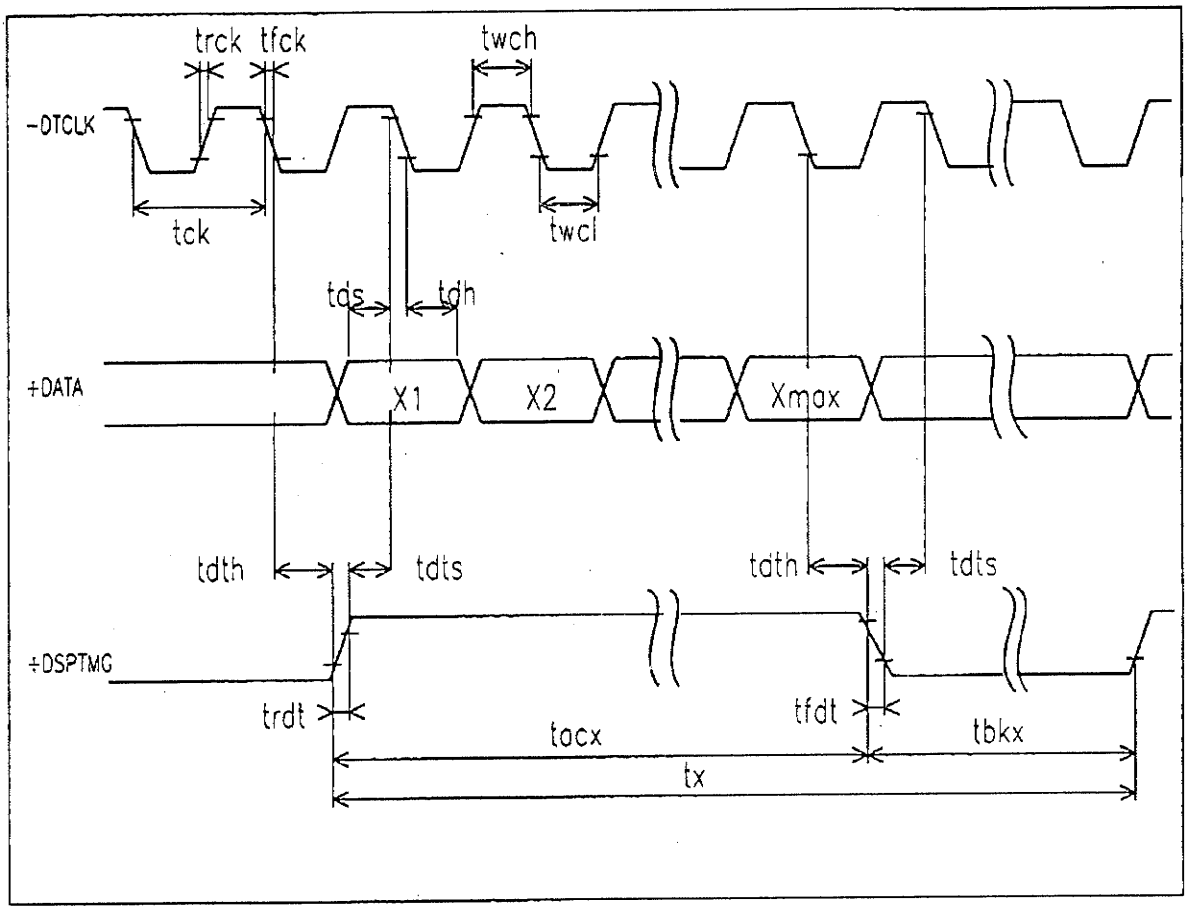
Basically ,interface timings should match the VESA 800 x 600 60Hz manufacturing-guide line timing.

Symbol	Signal Description	MIN	TYP	MAX	UNIT
f_{dck}	DTCLK Frequency	36.00	40.00	40.20	MHz
t_{ck}	DTCLK cycle time	27.77	25.00	24.88	nsec
t_{wcl}	DTCLK low width	5.00			nsec
t_{wch}	DTCLK high width	5.00			nsec
t_{rck}	DTCLK rise time			3.00	nsec
t_{fck}	DTCLK fall time			3.00	nsec
t_{ds}	Data setup time	5.00			nsec
t_{dh}	Data hold time	5.00			nsec
t_{rdt}	DSPTMG rise time	5.00			nsec

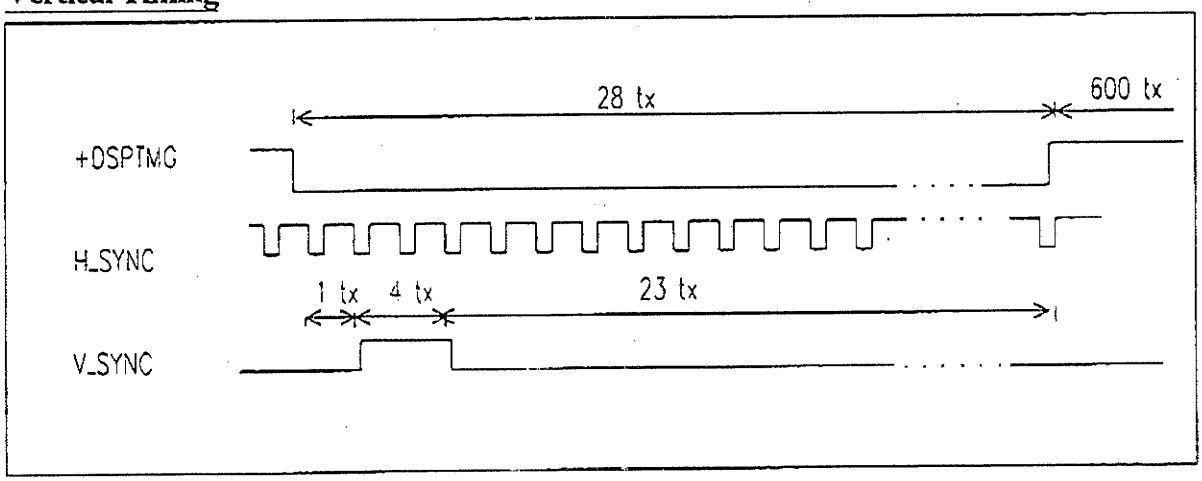
t_{fdt}	DSPTMG fall time	5.00			nsec
t_{dts}	DSPTMG setup time	5.00			nsec
t_{dth}	DSPTMG hold time	5.00			nsec
t_x	X total time	848	1056	1088	t_{ck}
t_{acx}	X active time		800		t_{ck}
t_{bkx}	X blank time	48	256		t_{ck}
H_{fp}	Hsync Front Porch	8	40		t_{ck}
H_{bp}	Hsync Back Porch	8	88		t_{ck}
H_w	H-sync width	8	128		t_{ck}
H_{sync}	H-frequency	35.16	37.88	38.46	KHz
t_y	Y total time	611	628	1013	t_x
t_{acy}	Y active time		600		t_x
V_{sync}	Frame rate	56.25	60.00	61.00	Hz
V_w	V-sync width	1	4	7	t_x
V_{fp}	V-sync front porch	1	1		t_x
V_{bp}	V-sync back porch	9	23	29	t_x

Preliminary

Horizontal Timing



Vertical Timing



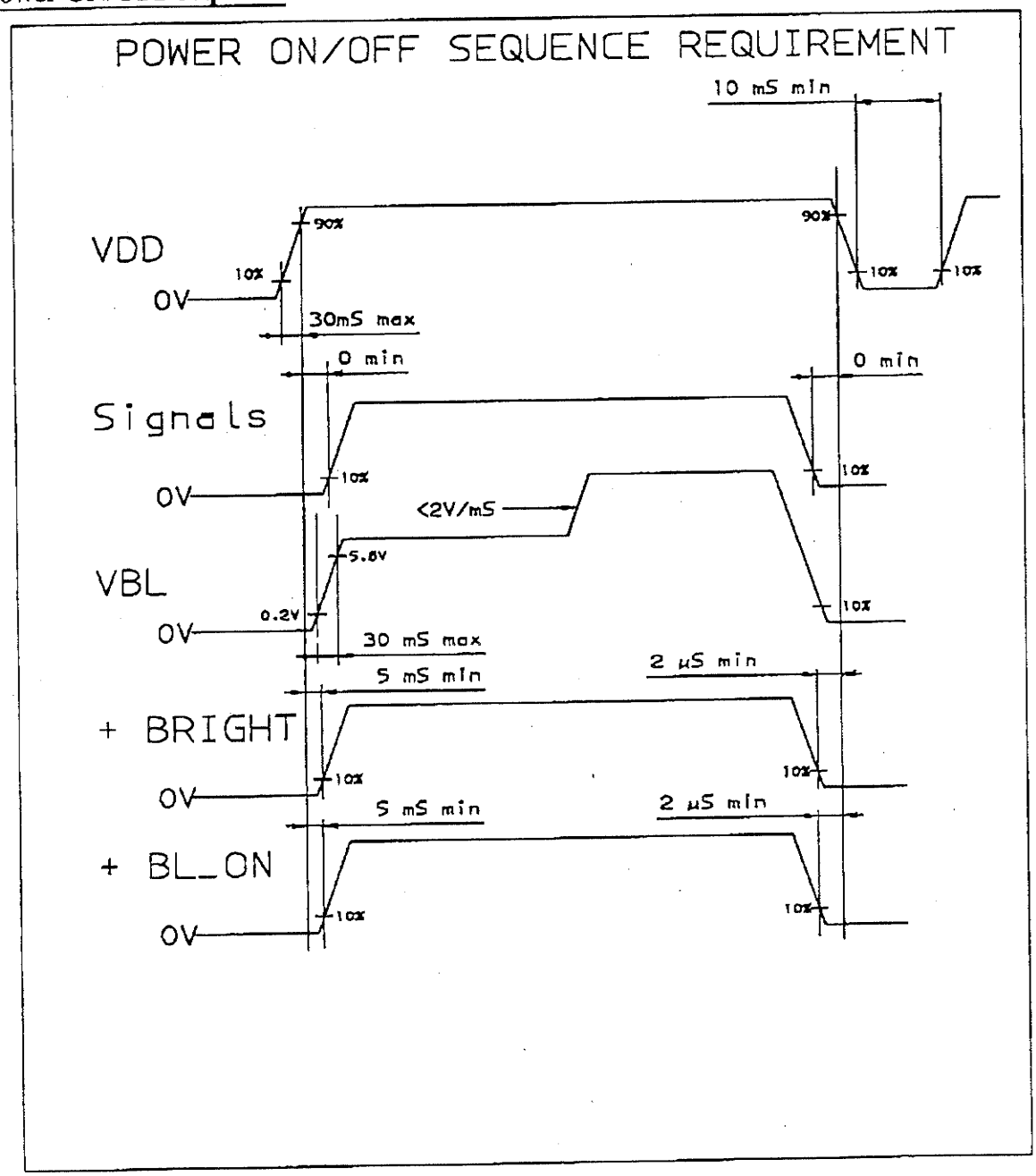
Preliminary

Power Requirement

SYMBOL	PARAMETER	Min.	Typ.	Max.	Unit	CONDITION
VDD	Logic/LCD Drive Voltage	+4.75	+5.0	+5.25	V	Load Capacitance 20uF
VBL(DC)	Backlight Voltage DC-mode	+6.5	+8.4/ +10.8		V	Battery Operation
VBL(AC)	Backlight Voltage AC-mode		+20.0/ +16.0	+21.0	V	AC Adapter Operation
PDD	VDD Power		0.63		W	AC Adapter Mode Battery Mode
PBL	VBL Power		3.90 2.80		W	AC Adapter Mode Battery Mode
PDD+PBL	Total Power		4.53 3.43		W	AC Adapter Mode Battery Mode
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			100	mVp-p	
VDDns	Allowable Logic/LCD Drive Ripple Noise			100	mVp-p	
VBLrp	Allowable Backlight Ripple Voltage			100	mVp-p	
VBLns	Allowable Backlight Ripple Noise			250	mVp-p	

Note: This requirements shall be met with 'All black pattern'.

Power ON/OFF sequence



Handling Precautions

1) Since front polarizer is easily damaged,pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately.Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled,wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or creak if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.

Reference Drawing - Refer Drawing P/N 46H3672 for details