For part NO. 26L4482
07K4086

Engineering Specification

13.3 inches XGA Color TFT/LCD Module
Model Name:ITXG75

Document Control Number : OEM75-01

Note:Specification is subject to change without notice. Consequently it is better to contact to IBM before proceeding with the design of your product incorporating this module.

Display Business Unit
International Business Machines Corporation

Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the CFL Reflector edge. Instead, press at the far ends of the CFL Reflector edge softly. Otherwise the TFT Module may be damaged.
10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bent the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.

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INTRODUCTION

Scope

This specification applies to the 13.3inches XGA Color TFT/LCD Module; ITXG75 designed for a display of notebook style personal computer.

The screen format is intended to support the XGA (1024(H) x 768(V)) screen and 262k colors (RGB 6-bit data driver).

All input signals are LVDS (Low Voltage Differential Signaling) interface compatible.

Applicability

This functional specification is applicable for the following devices.

LCD module P/N **25L8400** (ITXG75: LCD Module P/N w/o inverter card)

LCD module consists of the following components:

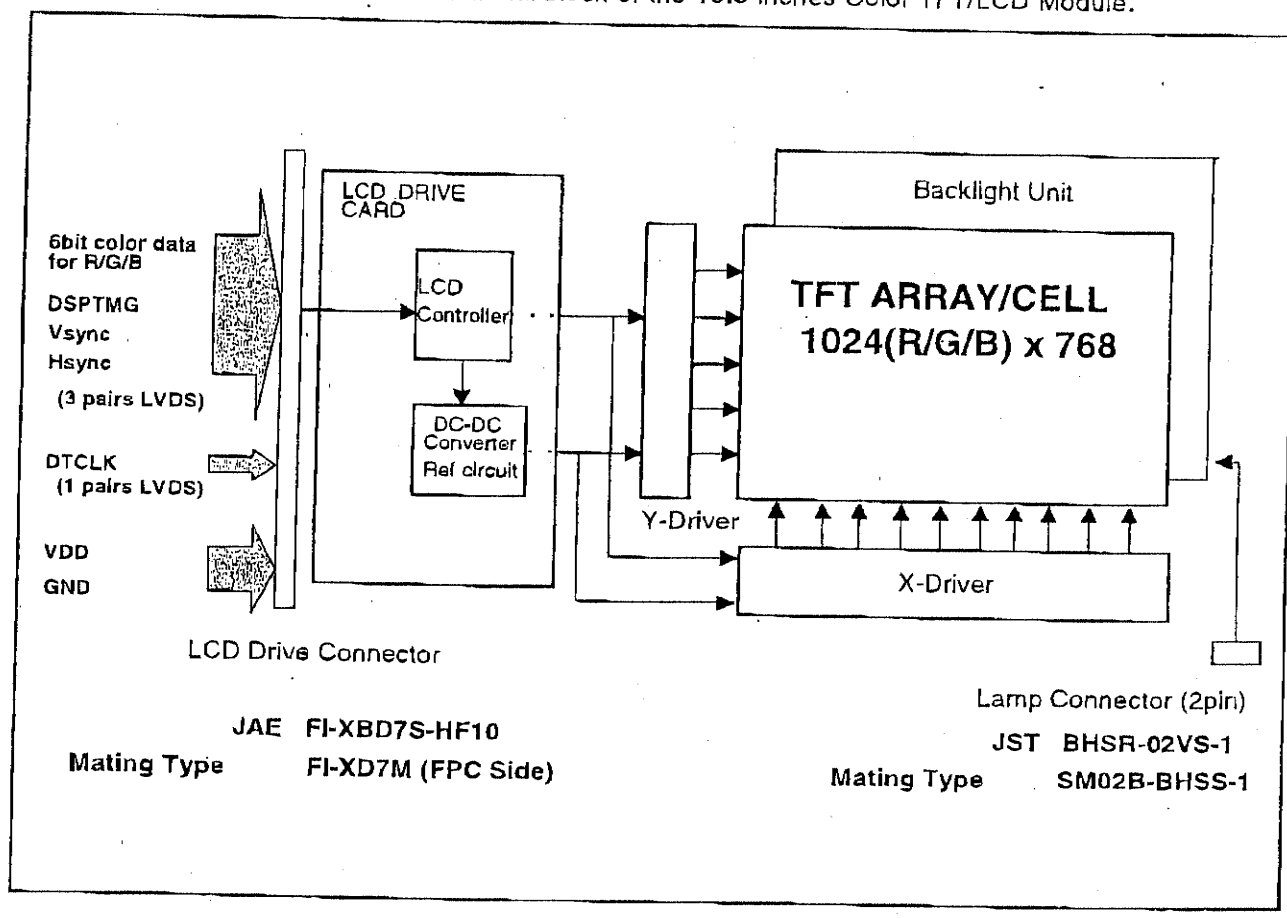
- A TFT displaying portion of a glass with an outer protective film.
- A back light unit using a Cold Cathode Fluorescent Lamp (CCFL).
- Associated electronics (drivers, control circuits, and DC-DC converter).
- A metal bezel and a plastic frame.

Quick Reference Table of Characteristics

	SPECIFICATIONS
Screen Diagonal	33.8mm (13.1")
Active Area	270.336mm x 202.752mm (H x V)
Pixels H x V	1024(x3) x 768
Pixel Pitch	0.264mm(per one triad) x 0.264mm
Pixel Arrangement	R.G.B. Vertical Stripe
Display Mode	Normally White
Typical White Luminance	125 [cd/m²] (Icfl=7mA)
Contrast Ratio	150 : 1 Typ.
Optical Rise Time/Fall Time [msec]	30msec Typ. ; 50ms Max.
Nominal Input Voltage (VDD)	+3.3 V
Typical Power Consumption (All Black Pattern) VDD line VCFL line	 1.3W 3.2W
Weight	395g Typ.
Physical Size	292mm x 215mm x 5.4mm (W x H x D)
Electrical Interface	R/G/B Data, 3 Sync, Signals, Clock (4 pairs LVDS)
Support Color	Native 262K colors (RGB 6-bit data driver)
Temperature Range Operating Storage (Shipping)	 0 ℃ to +50 ℃ -20 ℃ to +60 ℃

Functional Block Diagram

The following diagram shows the functional block of the 13.3 inches Color TFT/LCD Module.



SYSTEM INTERFACE

Physical Interface

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components or IBM approved types.

Signal Connector

Signal Connector

Connector Name / Designation	Signal Connector
Manufacturer	JAE
Type / Part Number	FI-XBD7S-HF10
Mating Type / Part Number	FI-XD7M

Signal Connector Pin Assignment

Pin#	Signal Name	Pin#	Signal Name
1 (Shell)	LVDS GND	2	RxCLK+
3	RxCLK-	4 (Shell)	LVDS GND
5	RxIN2+	6	RxIN2-
7 (Shell)	LVDS GND	8	RxIN1+
9	RxIN1-	10 (Shell)	LVDS GND
11	RxIN0+	12	RxIN0-
13 (Shell)	LVDS GND	14	NC
15	Reserved (Mfg Use)	16 (Shell)	LVDS GND
17	VDD Return / GND	18	VDD Return / GND
19 (Shell)	LVDS GND	20	VDD
21	VDD	22 (Shell)	LVDS GND

Lamp Connector

Lamp Connector

Connector Name / Designation	Lamp Connector
Manufacturer	JST
Type / Part Number	BHSR-02VS-1
Mating / Part Number	SM02B-BHSS-1

Lamp Connector Pin Assignment

Pin#	Signal Name
1	Lamp High
2	Lamp Low

ELECTRICAL INTERFACE REQUIREMENTS

The module using a LVDS receiver SN75LVDS86DGG(Texas Instruments) or compatible. LVDS is a differential signal technology for LCD interface and high speed data transfer device. Transmitter shall be SN75LVDS84DGG(negative edge sampling) or compatible.

Interface Signals

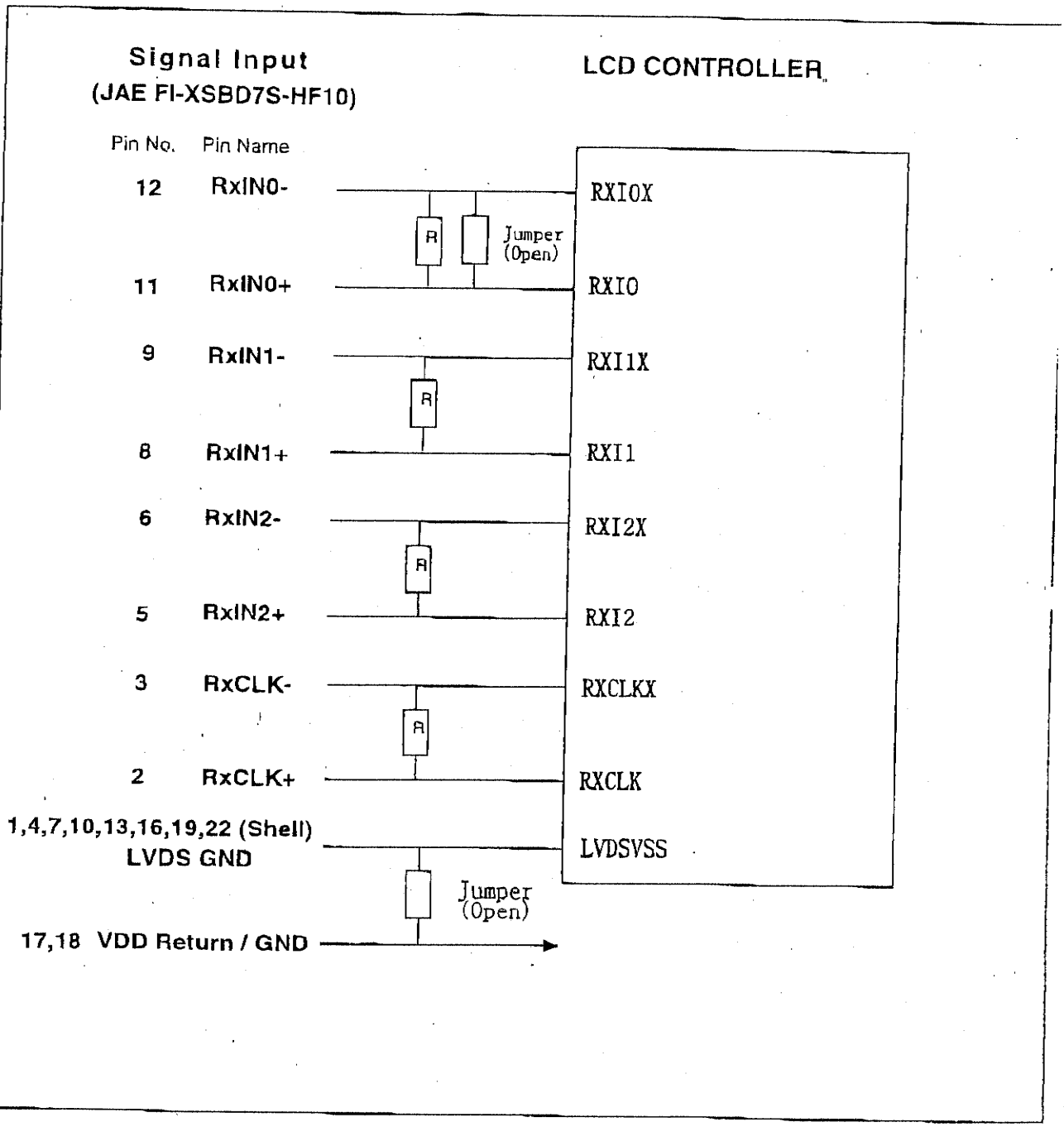
LCD Drive Connector Signal Description

LCD Driver Signal Description

PIN#	SIGNAL NAME	Description
1 (Shell)	LVDS GND	Connected to 'LVDS GND' pins of LVDS chip
2	RxCLK+	Positive LVDS differential clock input
3	RxCLK-	Negative LVDS differential clock input
4 (Shell)	LVDS GND	Connected to 'LVDS GND' pins of LVDS chip
5	RxIN2+	Positive LVDS differential data input (B2-B5, HSYNC,VSYNC,DSPTMG
6	RxIN2-	Negative LVDS differential data input (B2-B5, HSYNC,VSYNC,DSPTMG)
7 (Shell)	LVDS GND	Connected to 'LVDS GND' pins of LVDS chip
8	RxIN1+	Positive LVDS differential data input (G1-G5, B0-B1)
9	RxIN1-	Negative LVDS differential data input (G1-G5, B0-B1
10 (Shell)	LVDS GND	Connected to 'LVDS GND' pins of LVDS chip
11	RxIN0+	Positive LVDS differential data input (R0-R5, G0)
12	RxIN0-	Negative LVDS differential data input (R0-R5, G0)
13 (Shell)	LVDS GND	Connected to 'LVDS GND' pins of LVDS chip
14	NC	Reserved
15	Reserved	Reserved for DBU Mfg Option
16 (Shell)	LVDS GND	Connected to 'LVDS GND' pins of LVDS chip
17	GND	VDD Return
18	GND	VDD Return
19 (Shell)	LVDS GND	Connected to 'LVDS GND' pins of LVDS chip
20	VDD	+3.3V Power Supply
21	VDD	+3.3V Power Supply
22 (Shell)	LVDS GND	Connected to 'LVDS GND' pins of LVDS chip

Internal Circuit

Internal circuit of LVDS inputs are as follows.



Input circuit of LVDS signals

The module uses a 100 ohm resistor between positive and negative data lines of each receiver input..

LCD Drive Signal Description

Signal Description

SIGNAL NAME	Description	
+RED5 +RED4 +RED3 +RED2 +RED1 +RED0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB) **Red-pixel Data**	Each red pixel's brightness data consists of these 6 bits pixel data.
+GREEN 5 +GREEN 4 +GREEN 3 +GREEN 2 +GREEN 1 +GREEN 0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB) **Green-pixel Data**	Each green pixel's brightness data consists of these 6 bits pixel data.
+BLUE 5 +BLUE 4 +BLUE 3 +BLUE 2 +BLUE 1 +BLUE 0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB) **Blue-pixel Data**	Each blue pixel's brightness data consists of these 6 bits pixel data.
-DTCLK	**Data Clock**	The typical frequency is 65.0 MHz. The signal is used to strobe the pixel data and DSPTMG signals. All pixel data shall be valid at the falling edge when the DSPTMG signal is high.
DSPTMG	**Display Timing**	This signal is strobed at te falling edge of -DTCLK. When the signal is high, the pixel data shall be valid to be displayed.
VSYNC	**Vertical Sync**	The signal is synchronized to -DTCLK .
HSYNC	**Horizontal Sync**	The signal is synchronized to -DTCLK .

Note: Output signals from any system shall be low or Hi-Z state when VDD is off.

Pixel Data

The relations between pixel data and gray level are follows.

Signal Description

+RED 5 +GREEN 5 +BLUE 5	+RED 4 +GREEN 4 +BLUE 4	+RED 3 +GREEN 3 +BLUE 3	+RED 2 +GREEN 2 +BLUE 2	+RED 1 +GREEN 1 +BLUE 1	+RED 0 +GREEN 0 +BLUE 0	Gray Level
H	H	H	H	H	H	63
H	H	H	H	H	L	62
H	H	H	H	L	H	61
H	H	H	H	L	L	60
H	H	H	L	H	H	59
H	H	H	L	H	L	58
H	H	H	L	L	H	57
H	H	H	L	L	L	56
:	:	:	:	:	:	:
H	L	L	L	L	H	33
H	L	L	L	L	L	32
L	H	H	H	H	H	31
:	:	:	:	:	:	:
L	L	L	L	H	L	2
L	L	L	L	L	H	1
L	L	L	L	L	L	0

Signal Electrical Characteristics for LVDS(*)

Each signal characteristics are as follows;

Parameter	Condition	Min	Max	unit
Vth	Differential Input High Voltage(Vcm=+1.2V)		100	mV
Vtl	Differential Input Low Voltage(Vcn=+1.2V)	-100		mV

(*) It is recommended to refer the specifications of SN75LVDS86DGG (Texas Instruments) in detail.

Interface Timings (Output timings of SN75LVDS86DGG)

Basically, interface timings described here is not actual input timing of LCD module but output timing of SN75LVDS86DGG (Texas Instruments) or equivalent.

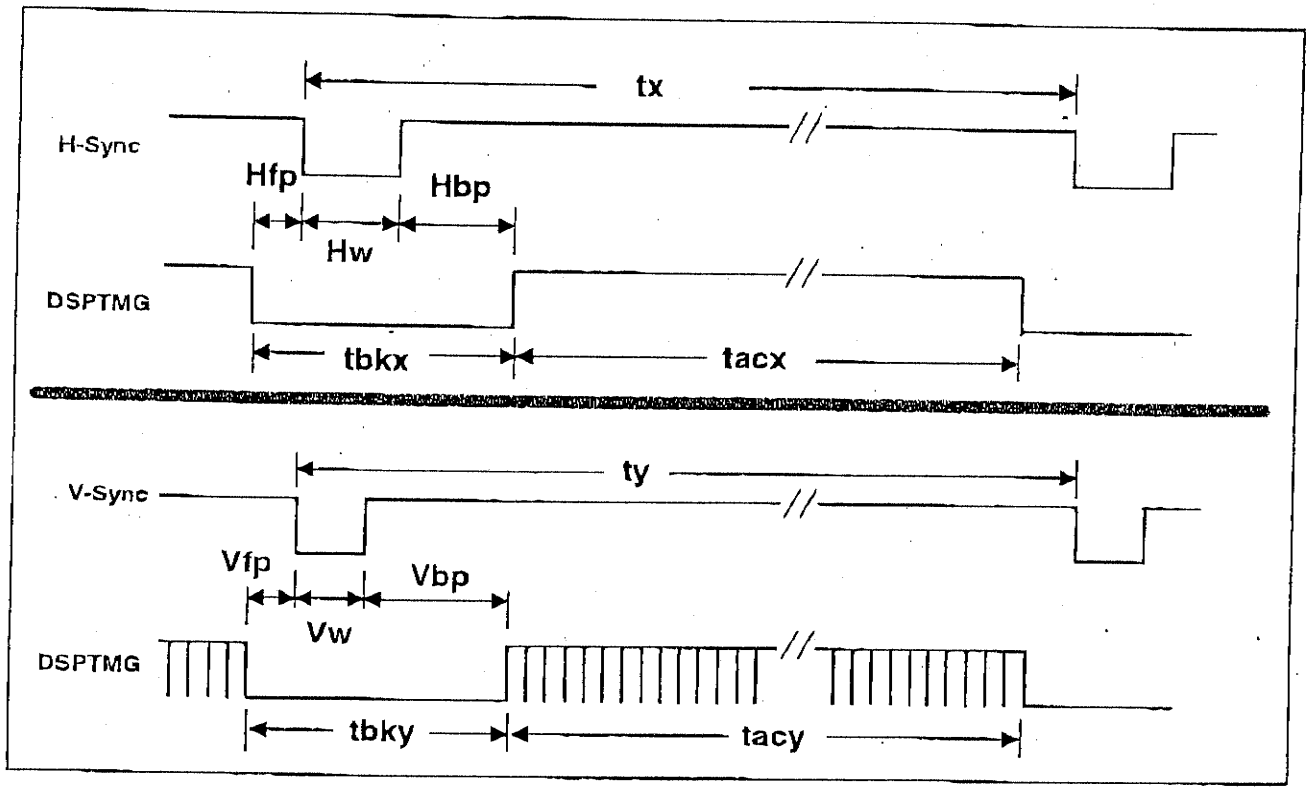
Timing Characteristics

Timing Characteristics

Symbol		MIN	TYP	MAX	Unit
f_{dck}	DTCLK Frequency		65.00	67.00	MHz
t_{ck}	DTCLK cycle time		15.38		nsec
t_x	X total time	1206	1344	2047	tck
t_{acx}	X active time	129	1024		tck
t_{bkx}	X blank time	90	320		tck
H_{fp}	H-sync front porch	0	24		tck
H_w	H-sync width	2	136		tck
H_{bp}	H-sync back porch	1	160		tck
H_{sync}	H-frequency		48.36		kHz
t_y	Y total time	771	806	1023	tx
t_{acy}	Y active time		768		tx
t_{bly}	Y blank time		38		tx
V_{sync}	Frame rate	(55)	60.00	61.00	Hz
V_{fp}	V-sync front porch	1	3		tx
V_w	V-sync width	1	6		tx
V_{bp}	V-sync back porch	7	29	63	tx

Note: H_w (H-sync width) + H_{bp} (H-sync back porch) should be less than 515 tck.

Timing Chart



Input Powers

Power Specifications

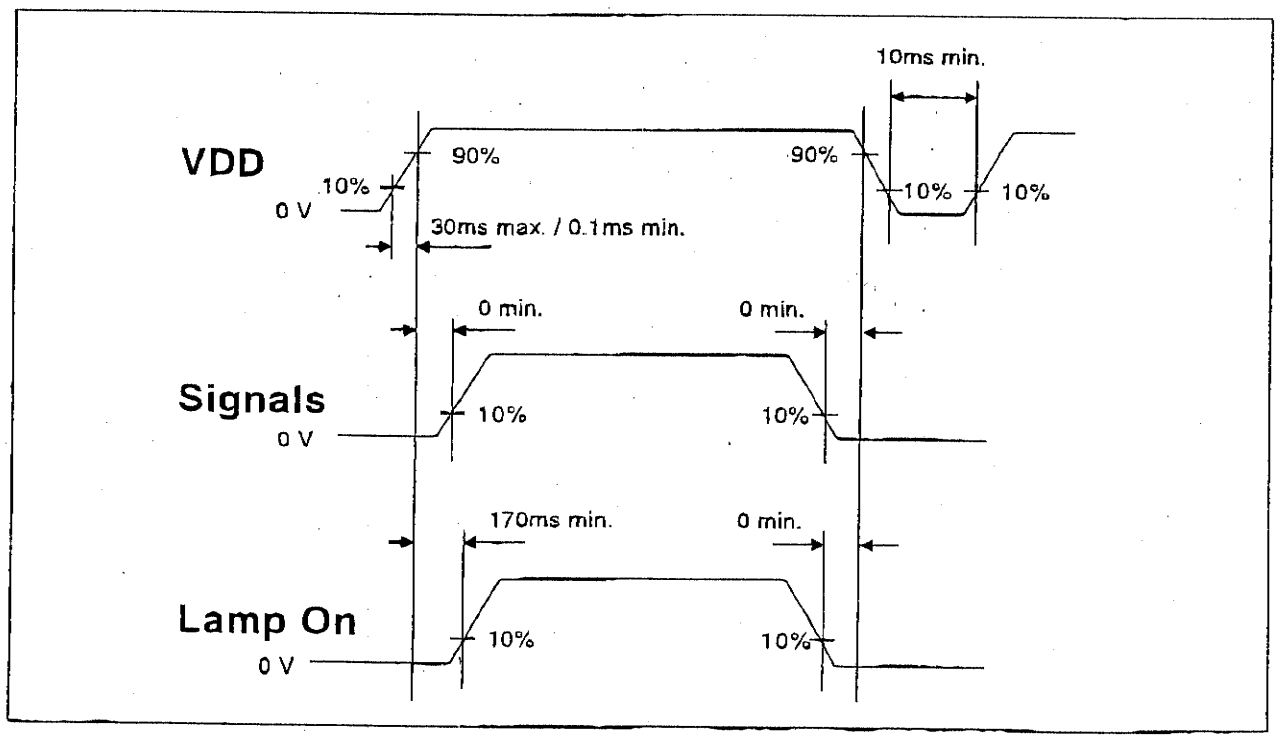
Input power specifications are as follows;

Power Requirements

SYMBOL	PARAMETER	Min	Typ	Max	UNITS	CONDITION
VDD	Logic/LCD Drive Voltage	3	3.3	3.6	V	Load Capacitance 100uF typ
PDD	VDD Power		1.3	1.4	W	All Black Pattern (VDD=3.3)
PDDmax	PDD Max			1.5	W	Sub-pixel Checker (VDD=3.6)
IDD max	IDD Max			500	mA	Sub-pixel Checker (VDD=3.0)
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			100	mVp-p	
VDDns	Allowable Logic/LCD Drive Ripple Noise			100	mVp-p	

Power On/Off Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



VDD/Signals Power On/Off Sequence Requirements

Power Specification of CFL / Design Point

Following is guideline for inverter;

CFL Specification and Design Point

Symbol	PARAMETER	MIN Note2	DP Note1	MAX Note2	UNITS	CONDITION	Note
(L63)	White Luminance	-	125	-	cd/m2	Ta=25℃	
ICFL	CFL current	3.0	7.0	7.2	mArms	Ta=25℃	
ICFLp	CFL Peak Inrush current	-	-	20	mA	Ta=25℃	2
fCFL	CFL Frequency	30	40	70	KHz	Ta=25℃	3
ViCFL	CFL Ignition Voltage	680			Vrms	Ta= 0℃	
VCFL	CFL Discharge Voltage (Reference)		460		Vrms	Ta=25℃	4
PCFL	CFL Power consumption		3.2		W	Ta=25℃	4

Note

1. Design Point ; At White Luminance 125 cd/m², PCFL=3.2 W is required.
2. duration=50 (msec)
3. CFL Frequency should be carefully determined to avoid interference between inverter and TFT LCD
4. Calculator value for reference (ICFL×VCFL=PCFL)

Absolute Maximum Ratings

Absolute maximum ratings of the module is as follows;

Absolute Maximum Ratings

SYMBOL	PARAMETER	VALUE	UNITS	CONDITION
VDD	Logic/LCD Drive Voltage	-0.3 to +4.6	V	
ViCFL	CFL Ignition Voltage	1,500	Vrms	Ta= 0℃
ICFL	CFL Current	7.2	mArms	

Color

The color point of each color element which is defined as the C.I.E. 1931 x,y coordinate readings on each primary color through the center of the screen, is given in the table shown below.

Chromatically

Color	x	y
Red	0.577	0.338
Green	0.310	0.563
Blue	0.158	0.157

White Balance

White balance defined as the C.I.E. 1931 x,y coordinate readings on each primary color through the center of the screen, is given in the table shown below.

White Balance

	Value
x	0.310
y	0.346

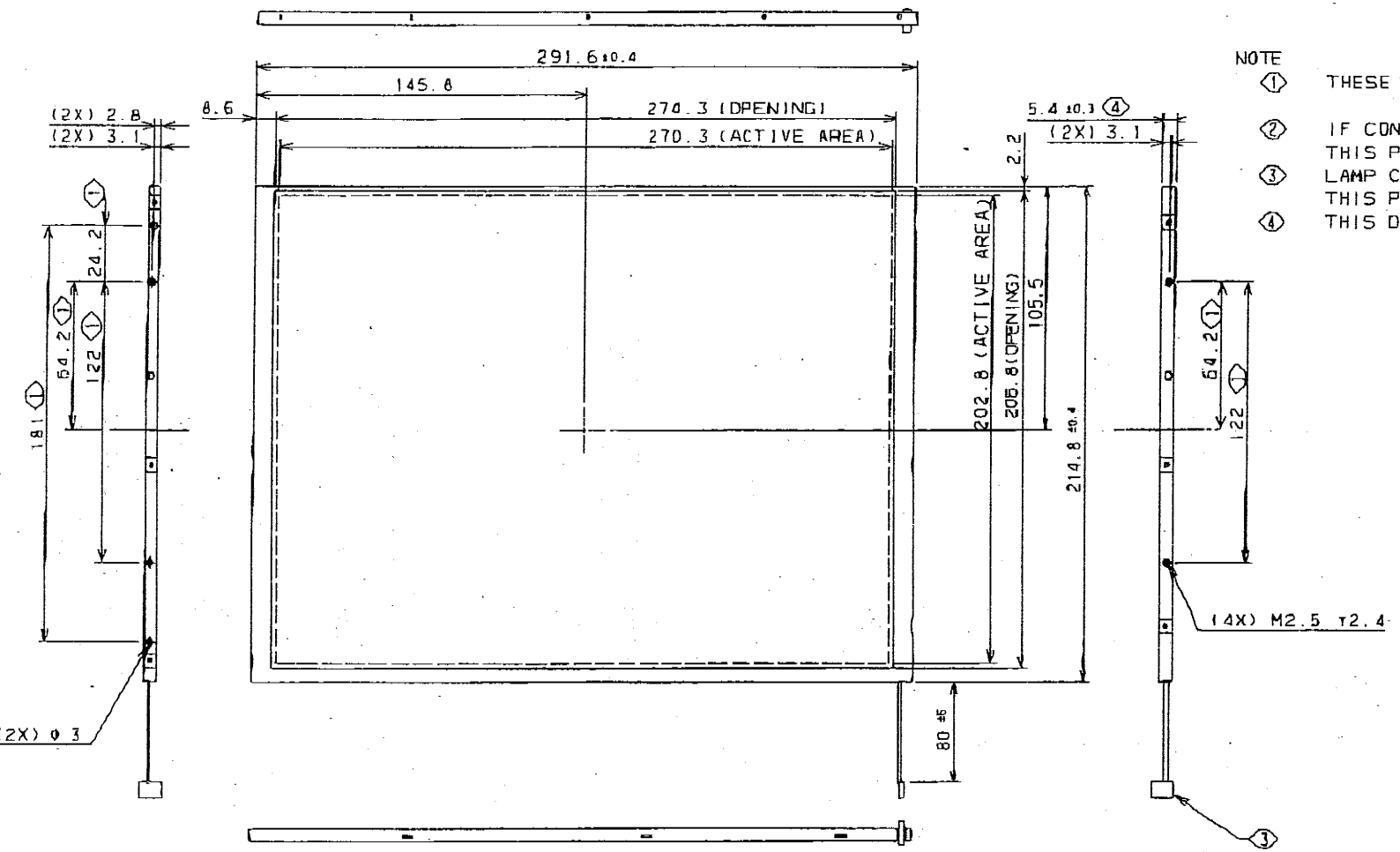
Refer to the attached drawing P/N25L8402.

****** End Of Page ******

REL FOR ASN	QTY	TECHNICAL APPROVAL				DATE	EC NO.		DATE	EC NO.
		ELECTRICAL			REL	14AUG98	F41440			
		MATERIAL				23JUL99	F41441			

PART NO. 25L8402

DEVELOPMENT NO. D/M



NOTE

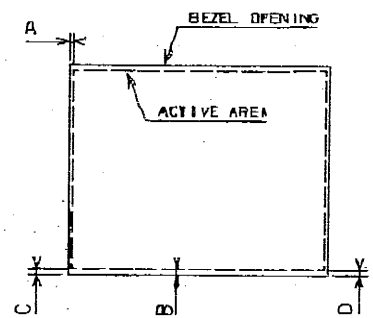
① THESE HOLES TO BE USED FOR FIXING PANEL.

② IF CONNECTOR TO BE JAE CO.,LTD.
THIS PART NUMBER TO BE "FX-XBD75-HF10".

③ LAMP CONNECTOR TO BE JST CO.,LTD.
THIS PART NUMBER TO BE "BHSR-02VS-1".

④ THIS DIMENSION EXCLUDES DEFORMATION.

BEZEL OPENING/DISPLAY POSITION



TOLERANCE X-DIRECTION A:2.0±0.8
TOLERANCE Y-DIRECTION B:2.0±0.8
OBLIQUITY OF DISPLAY AREA |C-D|<0.8

IBM MATERIAL NO.		MUST CONFORM TO ENG SPEC:8DX2324			SCALE: 1/1	PART NO. 25L8402	IBM
					0 mm 25 THIRD ANGLE PROJECTION	TITLE REF DWG	
MATL ALTERNATE NO.		TOLERANCES UNLESS NOTED				F8575	
		LINEAR ±		0.2		DESIGNER	M M 14 AUG 98
CASE DEPTH		ANGLES ±				CHECKED	K H 14 AUG 98
HARDNESS		RADII UNLESS NOTED				APPROVED	Y I 14 AUG 98
SURFACE TREATMENT	CODE NO.	EDGE/CORNER BREAKS	OUTSIDE MAX			CLASS	Y I 14 AUG 98
			INSIDE MAX				

ATE	EC NO.		DATE	EC NO.	PART NO. 25L8402	
4AUG98	F41440					
3JUL99	F41441				DEVELOPMENT NO.	O/M

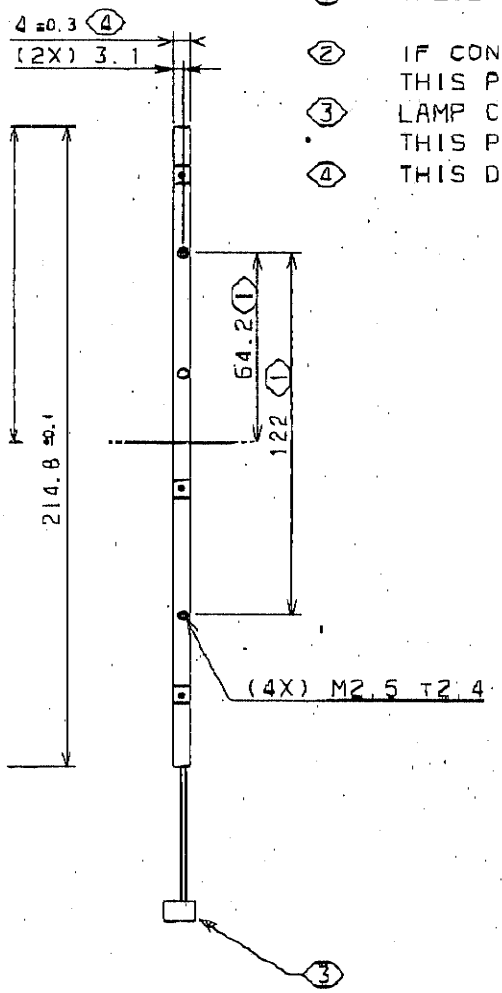
NOTE

① THESE HOLES TO BE USED FOR FIXING PANEL.

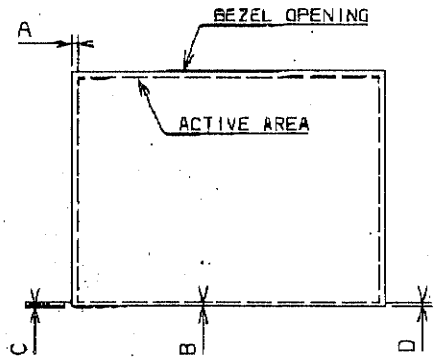
② IF CONNECTOR TO BE JAE CO.,LTD.
THIS PART NUMBER TO BE "FX-XBD7S-HF10".

③ LAMP CONNECTOR TO BE JST CO.,LTD.
THIS PART NUMBER TO BE "BHSR-02VS-1".

④ THIS DIMENSION EXCLUDES DEFORMATION.



BEZEL OPENING/DISPLAY POSITION



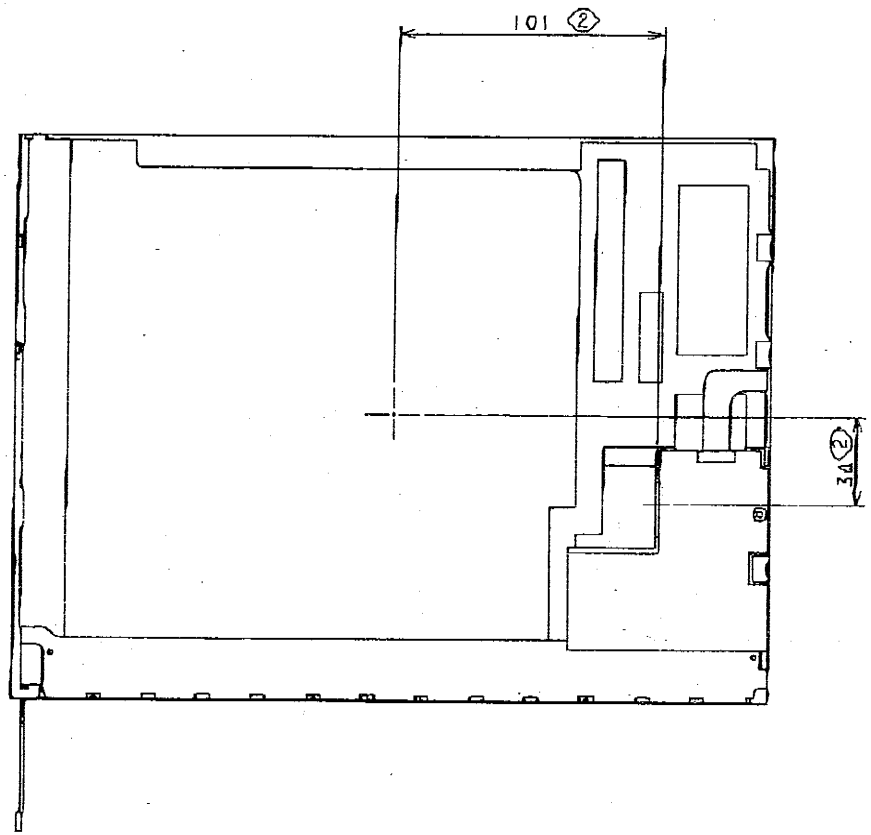
TOLERANCE X-DIRECTION A:2.0±0.8
TOLERANCE Y-DIRECTION B:2.0±0.8
OBLIQUITY OF DISPLAY AREA |C-D|<0.8

FORM TO ENG SPEC:80X2324		SCALE: 1/1	PART NO. 25L8402	IBM
ES UNLESS NOTED	SI	0 mm 25	TITLE REF DWG.	

REL FOR ASH	QTY	TECHNICAL APPROVAL		DATE	EC NO.		DATE	EC NO.
		ELECTRICAL	REL	14AUG98	F41440			
		MATERIAL		23JUL99	F41441			

PART NO. 25L8402

DEVELOPMENT NO.



IBM MATERIAL NO.		MUST CONFORM TO ENG SPEC: 80X2324		SCALE: 1/1	PART NO. 25L8402
				0 mm 25	TITLE REF DWG
MATL ALTERNATE NO. *		TOLERANCES UNLESS NOTED		THIRD ANGLE PROJECTION	F8575
		LINEAR ±	0.2		DESIGNER M M 14 AUG 98
CASE DEPTH		ANGLES ±			CHECKED K H 14 AUG 98
HARDNESS		RADII UNLESS NOTED			APPROVED Y I 14 AUG 98
SURFACE TREATMENT	CODE NO.	EDGE/CORNER BREAKS	OUTSIDE MAX		CLASS Y I 14 AUG 98
			INSIDE MAX		

SHEET 2 OF 2
25L8402