NEC

TFT COLOR LCD MODULE

Type: NL160120AC27-01
54cm (21.3 Type), UXGA
Analog, Full-color

SPECIFICATIONS

First edition

PRELIMINARY

This document is preliminary. All information in this document is subject to change without prior notice.

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Application examples recommended by NEC Corporation

Standard: Computer, Office equipment, Communication equipment, Test and Measurement equipment, Machine tools, Industrial robots, Audio and Visual equipment, Other consumer products, etc.

Special : Automotive and Transportation equipment, Traffic control systems, Antidisaster systems, Anticrime systems, etc.

CONTENTS

1. DESCRIPTION

NL160120AC27-01 is a TFT(thin film transistor) active matrix color liquid crystal display(LCD) comprising amorphous silicon TFT attached to each signal electrode, a driving circuit and a backlight. NL160120AC27-01 has a built-in backlight with an inverter.

The 54cm(21.3" Type) diagonal display area contains 1600 × 1200 pixels and can display full-color (more than 16 million colors simultaneously). Also, it has wide viewing angle and multi-scan function. Therefore, this module is so called Super Fine TFT.

2. FEATURES

- Ultra wide viewing angle with lateral electric field.
- High luminance and Low reflection
- Analog RGB signals
- Multi-scan function: e.g., UXGA, SXGA, XGA, SVGA, VGA, VGA-TEXT, MAC, SUN, IBM VGA
- Direct type backlight (Twelve lamps, an Inverter)
- Backlight unit replaceable (Type No. : 213LHS01)
- On Screen Display
- Application with the OSD function might conflict with patents in Europe and/or the U.S.A. If you apply the OSD function appreciate the patents at your side.

VESA:	Video Electronics Standards Association
DPMS:	Display Power Management Signaling
DDC1:	Display Data Channel 1
DDC2B:	Display Data Channel 2B

3. APPLICATIONS

- Engineering work stations, Desk-top type of PCs
- Display terminals for control system
- Monitors

4. STRUCTURE AND FUNCTIONS

A color TFT (thin film transistor) LCD module is comprised of a TFT liquid crystal panel structure, LSIs for driving the TFT array, and a backlight assembly. Sandwiching liquid crystal material in the narrow gap between a TFT array glass substrate and a color filter glass substrate creates the TFT panel structure. After the driver LSIs are connected to the panel, the backlight assembly is attached to the backside of the panel.

RGB (red, green, blue) data signals from a source system is modulated into a form suitable for active matrix addressing by the onboard signal processor and sent to the driver LSIs which in turn addresses the individual TFT cells.

Acting as an Electro-optical switch, each TFT cell regulates light transmission from the backlight assembly when activated by the data source. By regulating the amount of light passing through the array of red, green, and blue dots, color images are created with clarity.

5. OUTLINE OF CHARACTERISTICS (at room temperature)

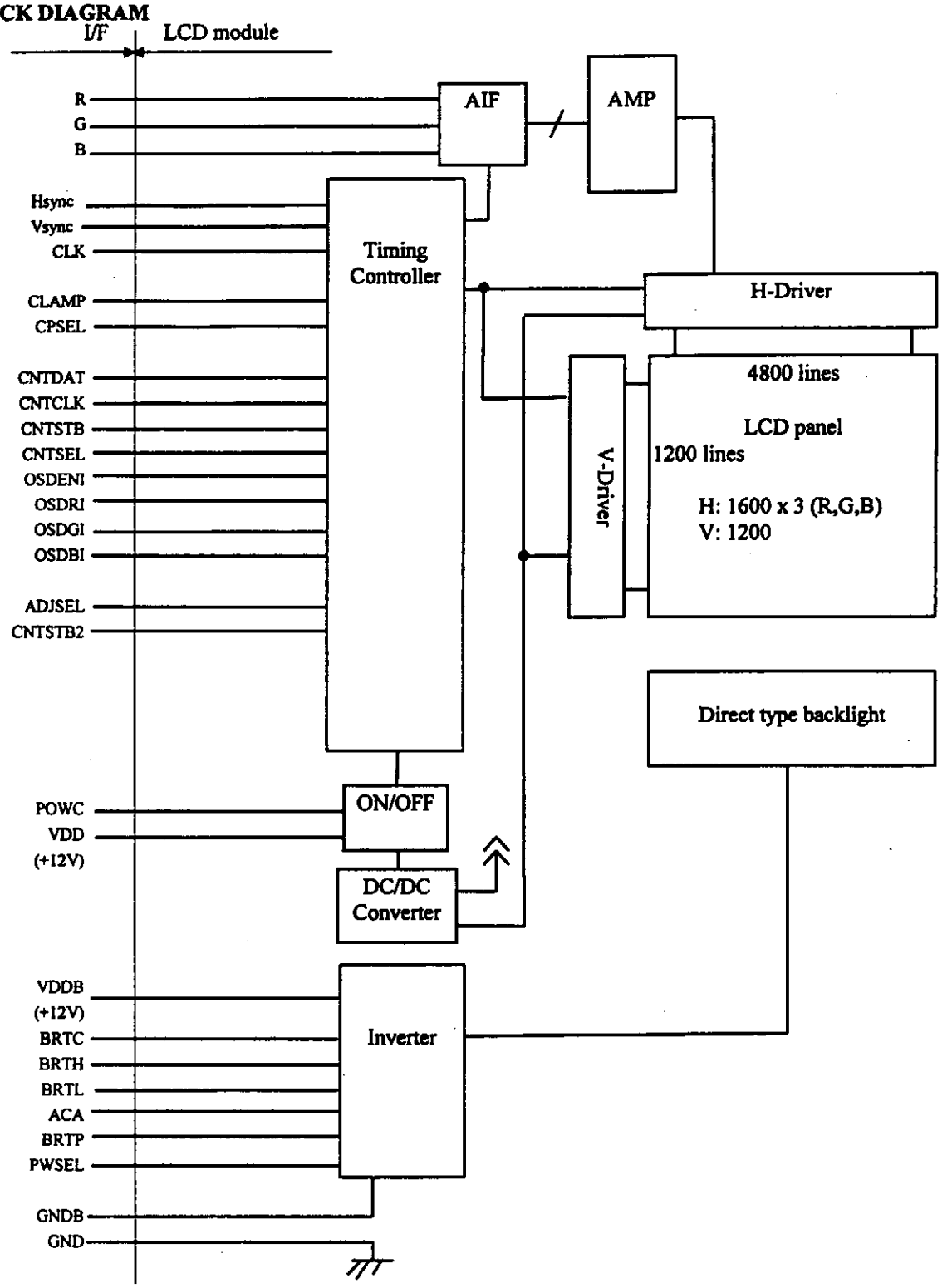
Display area	432.0 (H) × 324.0 (V)mm
Drive system	a-Si TFT active matrix
Display colors	full-color
Number of pixels	1600 × 1200
Pixel arrangement	RGB vertical stripe
Pixel pitch	0.270 (H) × 0.270 (V)mm
Module size	470.0 (H) × 382.0 (V) × 41.6 typ. (D) mm
Weight	2900 g(typ.)
Contrast ratio	250:1(typ.)

Viewing angle (more than the contrast ratio of 10:1)
- Horizontal: 85 ° (typ. , left side, right side)
- Vertical: 85 ° (typ. , up side, down side)

Optimum grayscale (γ =2.2): perpendicular

Pencil hardness	3 H (min. JIS K5400)
Color gamut	60 %(typ. At center, To NTSC)
Response time	40 ms(typ.), " black " to " white "
Luminance	200 cd/m^2(typ.)
Signal system	Analog RGB signals, Synchronous signals(Hsync, Vsync), Dot clock(CLK)
Supply voltage	12 V, 12 V (Logic, LCD driving, Backlight)
Backlight	Direct type: Eight cold cathode fluorescent lamps with inverter 〈Replacement parts〉 Inverter Parts No. : 213PW011 Backlight unit Parts No. : 213LHS01
Power consumption	69.6 W(typ.)

6. BLOCK DIAGRAM



Note 1: GND is connected to Frame (FG).
GNDB is not connected to GND.

7. SPECIFICATIONS

7.1 GENERAL SPECIFICATIONS

Items	Contents	Unit
Module size	470.0±1.0 (H) x 382.0±1.0 (V) x 42.5 (max.)(D)	mm
Display area	432.0 (H) x 324.0 (V)	mm
Number of dots	1600 x 3 (H) x 1200 (V)	dots
Pixel pitch	0.270 (H) x 0.270 (V)	mm
Dot pitch	0.090 (H) x 0.270 (V)	mm
Pixel arrangement	RGB (Red, Green, Blue) vertical stripe	–
Display colors	Full color	Color
Weight	2900 (typ.) 3000 (max.)	g

7.2 ABSOLUTE MAXIMUM RATINGS

Parameters	Symbols	Ratings	Unit	Remarks
Supply voltage	VDD	-0.3 to +14	V	Ta=25℃
	VDDB	-0.3 to +14	V	
Logic input voltage	Vin1	-0.3 to +5.5	V	Ta=25℃ VDD=12V
R,G, B input voltage	Vin2	-6.0 to +6.0	V	
CLK input voltage	Vin3	-7.0 to +7.0	V	
BRTL input voltage	Vin4	-0.3 to +1.5	V	
Storage temp.	Tst	-20 to +60	℃	–
Operating temp.	Top	0 to +50	℃	Module surface Note 1
Humidity Note 2	≦95% relative humidity			Ta≦40 ℃
	≦85% relative humidity			40<Ta≦50 ℃
	Absolute humidity(g/m^3) shall not exceed Ta=50℃, 85% relative humidity level.			Ta>50 ℃

Note 1: Measured at the surface of LCD panel

Note 2: No condensation

7.3 ELECTRICAL CHARACTERISTICS

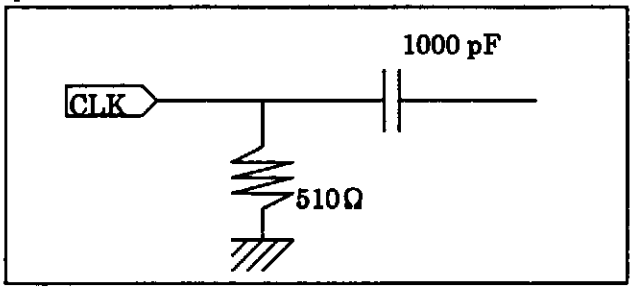
(1) Logic, LCD driving, Backlight

(Ta=25℃)

Items	Symbols	Min.	Typ.	Max.	Unit	Remarks
Supply voltage	VDD	11.4	12.0	12.6	V	for LCD driving
	VDDB	10.8	12.0	13.2	V	for backlight
Logic input " L " voltage	ViL1	0	–	0.8	V	
Logic input " H " voltage	ViH1	2.0	–	5.25	V	
CLK input voltage	ViCLK	0.6	–	1.0	Vp-p	for CLK
CLK DC input voltage	ViDC CLK	-4.5	–	+4.5	V	
Logic input " L " current 1	IiL1	-10	–	–	μA	for Hsync, Vsync
Logic input " H " current 1	IiH1	–	–	160	μA	
Logic input " L " current 2	IiL2	-900	–	–	μA	for CNTSEL, CPSEL, and POWC ADJDEL,
Logic input " H " current 2	IiH2	–	–	10	μA	
Logic input " L " current 3	IiL3	-10	–	–	μA	for CNTDAT, CNTSTB, CNTCLK, CNTSTB2
Logic input " H " current 3	IiH3	–	–	150	μA	
Logic input " L " current 4	IiL4	-10	–	–	μA	For CLAMP, OSDENI, OSDRI, OSDGI, OSDBI
Logic input " H " current 4	IiH4	–	–	1440	μA	
Logic input " L " current 5	IiL5	-1.6	–	–	mA	for BRTP
Logic input " H " current 5	IiH5	–	–	3.5	mA	
Logic input " L " current 6	IiL5	-610	–	–	μA	for BRTC, PWSEL
Logic input " H " current 6	IiH5	–	–	440	μA	
Supply current	IDDB	–	4200 note 1	5000	mA	for backlight VDDB=12.0V (Max. luminance)
	IDD	–	1600 note 1	2000	mA	for LCD driving VDD=12.0V

Note 1: The display is Dot- checkered pattern.

(2)CLK input equivalent circuit



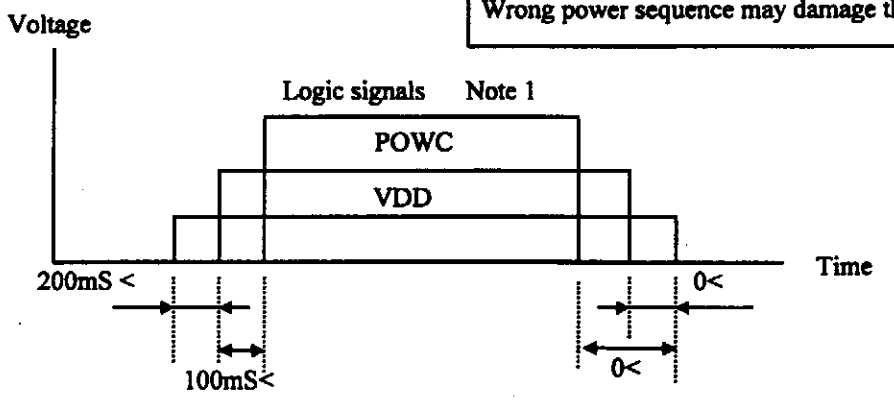
(3) Video signal (R, G, B) input

(Ta=25℃)

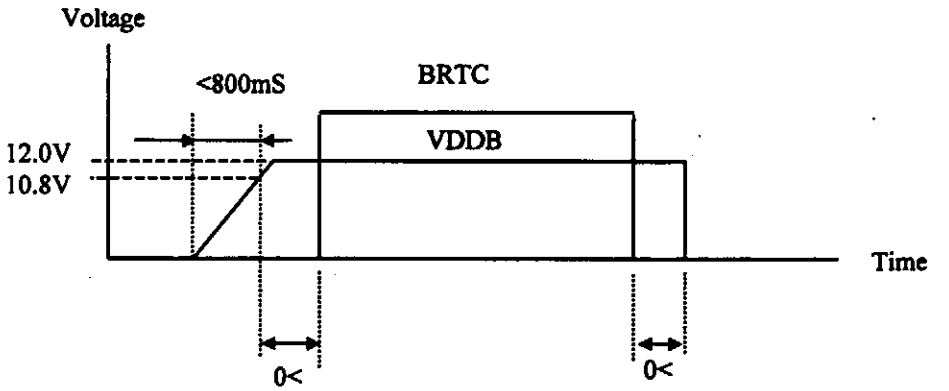
Items	Min.	Typ.	Max.	Unit	Remarks
Maximum amplitude (white – black)	0 (black)	0.7 (white)	0.9	Vp-p	Need to adjust contrast if input is more than 0.7Vp-p
DC input level (black)	-3.5	–	+3.5	V	–

7.4 POWER SUPPLY SEQUENCE

CAUTION
Wrong power sequence may damage the module.



Note 1: Synchronous signals, Control signals, CLK



(1) Logic signals (synchronous signals and control signals) should be "0" voltage (V), when VDD is not input. If input voltage to signal lines is higher than 0.3 V, the internal circuit will be damaged.

(2) LCD module will shut down the power supply of driving voltage to LCD panel internally, when one of CLK, Hsync, and Vsync is not input more than 90 ms typically.
As the display data are unstable in this period, the display maybe disordered. But the backlight works correctly even this period. So the backlight should be controlled by BRTC signal.

(3) The backlight ON/OFF (BRTC signal) should be controlled while logic signals are supplied. The backlight power supply (VDDB) is not related to the power supply sequence. However, unstable data will be displayed when the backlight power is turned ON with no logic signals.

(4) Keep POWC signal "L" more than 200 ms after the power supply (VDD) is input, if POWC signal is controlled.

(5) Analog RGB inputs are independent from this power supply sequence.

(6) The backlight is turned off with safety circuit, when "L" period of BRTP signal is input more than 50 ms or 12V for backlight is started up more than 800ms.

(7) Do not input "H" ACA and PWSEL, when VDD is 0V or BRTC is "L".

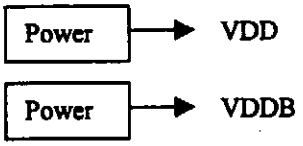
(8) Ripple of supply voltage

	VDD (for logic and LCD driver)	VDDB (for backligth)
Acceptable range	≦ 100 m Vp-p	≦ 200 m Vp-p

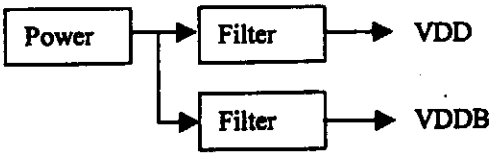
Note 1: The acceptable range of ripple voltage includes spike noise.

Example of the power supply connection

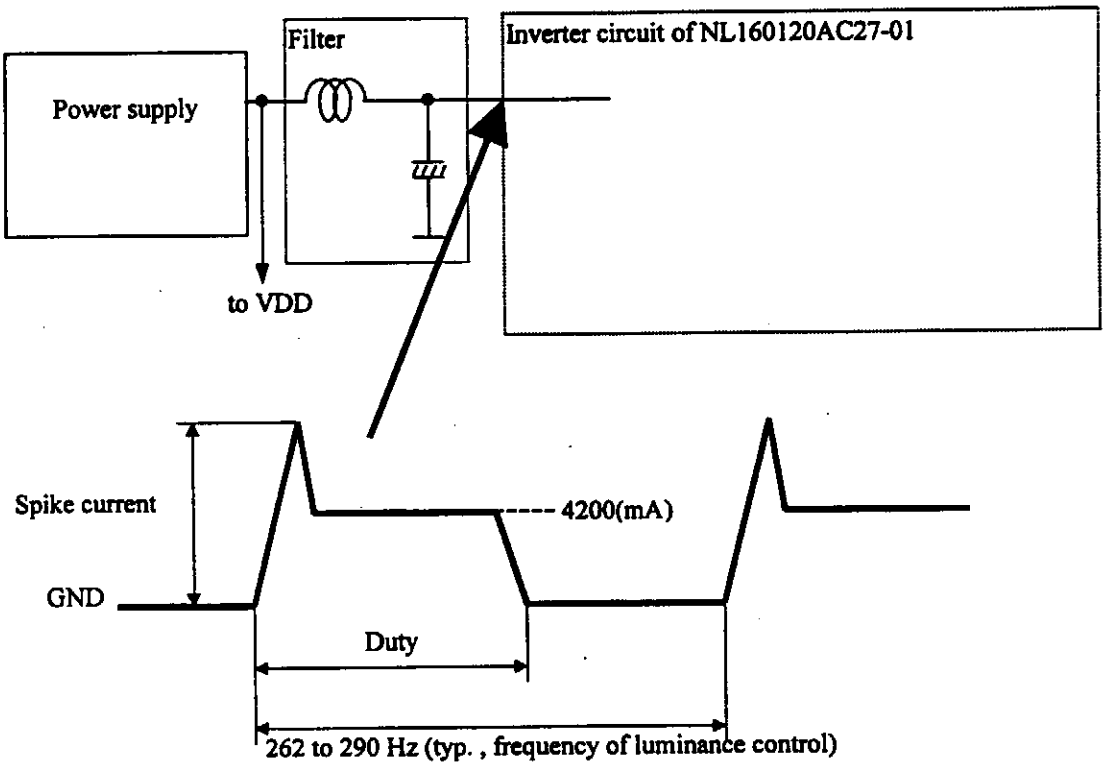
a) Separate the power supplies



b) Put the filters



(9) Inverter current wave



In the maximum luminance, the inverter current is DC. However, in the luminance control by BRTP signal, the above duty varies 100% to 20% and the spike current, which causes the noise on the screen, may be observed. In this case, adjust the value of the capacitance in the above filter to eliminate the noise on the screen.

(10) Fuse

Supply voltage	Part No.	Supplier	Ratings	Remarks
VDD	CCF1NTE4	KOA	4.0A	-
VDDB	R451007	Littlefuse Inc	7.0A	-

7.5 INTERFACE PIN CONNECTIONS

(1) CN1

Part No. : MRF03-6R-SMT

Adaptable socket : MRF03-2×6P-1.27(For cable type) or MRF03-6PR-SMT(For board to board type)

Supplier : HIROSE ELECTRIC CO., LTD. (coaxial type)

Pin No.	Symbols	Pin No.	Symbols
1	B	4	Vsync
2	G	5	Hsync
3	R	6 ▼	CLK

Figure from socket view

(2) CN2

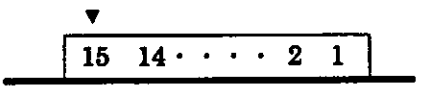
Part No. : IL-Z-15PL-SMTY

Adaptable socket : IL-Z-15S-S125C3

Supplier : Japan Aviation Electronics Industry Limited (JAE)

Pin No.	Symbols	Pin No.	Symbols
1	VDD	9	GND
2	VDD	10	CNTCLK
3	GND	11	CPSEL
4	GND	12	CLAMP
5	POWC	13	GND
6	CNTSEL	14	N.C.
7	CNTDAT	15 ▼	GND
8	CNTSTB		

Figure from socket view



Note 1:N.C. (No connection) must be open.

(3) CN3

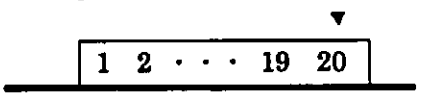
Part No. : DF14A-20P-1.25H

Adaptable socket : DF14-20S-1.25C

Supplier : HIROSE ELECTRIC CO., LTD. (coaxial type)

Pin No.	Symbols	Pin No.	Symbols
1	GND	11	ADJSEL
2	OSDENI	12	N.C.
3	GND	13	CNTSTB2
4	OSDBI	14	GND
5	GND	15	N.C.
6	OSDGI	16	GND
7	GND	17	N.C.
8	OSDRI	18	N.C.
9	GND	19	N.C.
10	N.C.	20 ▼	N.C.

Figure from socket view



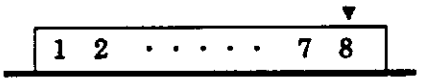
(4) CN201

Part No. : DF3-8P-2H
Adaptable socket: DF3-8S-2C
Supplier: HIROSE ELECTRIC CO., LTD.

Pin No.	Symbols	Pin No.	Symbols
1	GNDB	5	VDDB
2	GNDB	6	VDDB
3	GNDB	7	VDDB
4	GNDB	8 ▼	VDDB

note 1: N.C. (No connection) must be open.

Figure from socket view



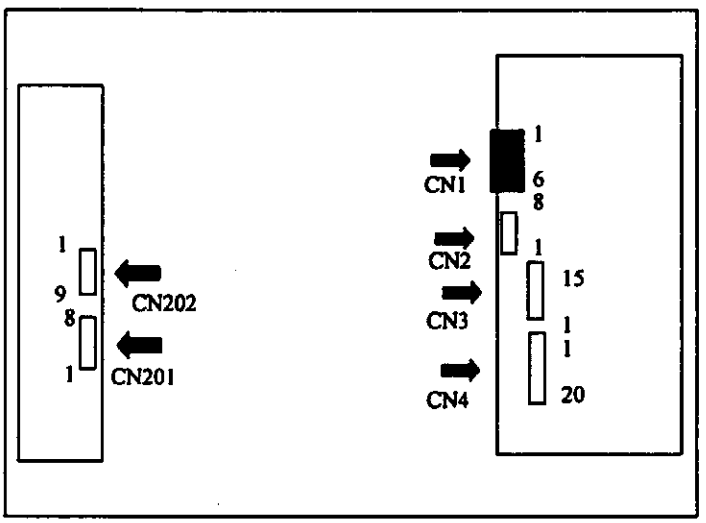
(5) CN202

Part No. : IL-Z-9PL1-SMTY
Adaptable socket: IL-Z-9S-S125C3
Supplier: Japan Aviation Electronics Industry Limited (JAE)

Pin No.	Symbols	Pin No.	Symbols
1	GNDB	6	BRTL
2	GNDB	7	BRTP
3	ACA	8	GNDB
4	BRTC	9 ▼	PWSEL
5	BRTH	-	

Figure from socket view

Rear view



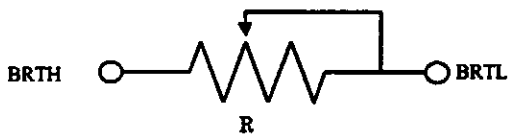
7.6 PIN FUNCTIONS

Symbols	I/O	Logic	Description
CLK	Input	Negative	Dot clock input. (ECL level) Timing signal for display data.
Hsync	Input	Negative	Horizontal synchronous signal input (TTL level)
Vsync	Input	Negative	Vertical synchronous signal input (TTL level)
R	Input	–	Red video signal input (0.7Vp-p, input impedance 75Ω)
G	Input	–	Green video signal input (0.7Vp-p, input impedance 75Ω)
B	Input	–	Blue video signal input (0.7Vp-p, input impedance 75Ω)
POWC	Input	Positive	Power control signal (TTL level) "H" or "open" : Logic and LCD powers are on. "L" : Logic and LCD powers are off. (Note 2)
CNTSEL	Input	–	Display control signal in case of serial communications.(TTL level) "H" or "Open" : Default "L" : External control Serial communications are set up by external control.
CNTDAT	Input	Positive	Display control data (TTL level) Detail of CNTDAT is mentioned in 7.7 **FUNCTIONS**.
CNTCLK	Input	Positive	CLK for display control data (TTL level) Detail of CNTCLK is mentioned in 7.7 **FUNCTIONS**.
CNTSTB	Input	Positive	Latch pulse for display control data (TTL level) Detail of CNTSTB is mentioned in 7.7 **FUNCTIONS**.
CPSEL	Input	–	Clamp function select signal (TTL level) "H" or "Open" : Default "L" : CLAMP signal is possible.(External control)
CLAMP	Input	Positive	Clamp timing signal of black level (TTL level) This mode works in CPSEL = "L".
BRTC	Input	Positive	Backlight ON/OFF control signal(TTL level) "H" or "Open" : Backlight on "L" : Backlight off
BRTH	Input	–	Backlight luminance control-1 Variable resistor control(Note 3) or voltage control (Note 4) These controls work in BRTP = "Open".
BRTL	Input	–	
BRTP	Input	–	Backlight luminance control-2 (TTL level) BRTP signal control (Note 5)
PWSEL	Input	–	Luminance control select signal (TTL level) "H" or "Open" : Variable resistor control or voltage control "L" : BRTP signal control
ADJSEL	Input	Positive	Contrast, brightness select control signal (TTL level) "H" or "Open" : Default "L" : External control Serial communications are set up by external control.

Symbols	I/O	Logic	Description
CNTSTB2	Input	Positive	Latch pulse2 for display control data Detail of CNTSTB2 is mentioned in **7.9 OSD FUNCTIONS.**
OSDRI	Input	–	OSD Red input (TTL level) Detail of OSDRI is mentioned in **7.9 OSD FUNCTIONS.**
OSDGI	Input	–	OSD Green input (TTL level) Detail of OSDGI is mentioned in **7.9 OSD FUNCTIONS.**
OSDBI	Input	–	OSD Blue input (TTL level) Detail of OSDBI is mentioned in **7.9 OSD FUNCTIONS.**
OSDENI	Input	Positive	OSD enable signal (TTL 0level) Detail of OSDENI is mentioned in **7.9 OSD FUNCTIONS.**
VDD	–	–	VDD (+12V±5%) power supply for logic and LCD driving.
VDDB	–	–	VDDB (+12V±5%) power supply for backlight. (Note 1)
GND	–	–	Ground for logic and LCD driving (VDD) GND is connected to the module GND (FG).
GNDB	–	–	Ground for backlight power supply (VDDB) GNDB is not connected to the module GND (FG).

Note 1: When POWC is "L", serial communication data is clear, please set again. When POWC is "L", logic input signal has to be all "0V". If more than "0.3V" is inputted, the LCD module may be broken.

Note 2: The way of luminance control by a variable resistor
This way works in PWSEL = "H" or "Open" and in BRTP = "Open". The variable resistor for luminance control should be 10kΩ type, and zero point of the resistor correspond to minimum luminance.



Mating variable resistor:
10KΩ±5%, B curve

Maximum luminance (100%): R= 10KΩ
Minimum luminance (30%; ACA="H", 60%; ACA="L"): R= 0Ω

Note 4: The way of luminance control by voltage
This way works in PWSEL = "H" or "Open" and in BRTP = "Open". If luminance is controlled with BRTH/BRTL input voltage, at first BRTH is "0V", and BRTL input voltage controls luminance. When BRTL input voltage is "1V", the luminance becomes maximum, and when BRTL input voltage is "0V", the luminance becomes minimum.

Maximum luminance (100%): BRTL="1V"
Minimum luminance (30%; ACA="H", 60%; ACA="L"): BRTL="0V"

Note 5: The way of luminance control with BRTP signal
Detail of **7.10 OUTSIDE CONTROL FOR LUMINANCE**

7.7 FUNCTIONS

This LCD module has following functions by serial data input (table 1)

(1) Expansion mode:	See table 2 and **7.8 EXPANSION FUNCTIONS**
(2) Control Display position (VERTICAL):	See table 3
(3) Control Display position (HORIZONTAL):	See table 6
(4) Control CLK delay:	See table 4
(5) Change CLK fall/rise synchronous:	See table 5
(6) Sub-Contrast control:	See table 9, 10 and **7.8.4 COLOR CONTROL FUNCTION AND GRAPH IMAGE**
(7) Sub-Brightness control:	

Set up the following items to work the above functions

(A) CLK counts of horizontal period:	See table 7
(B) CLK frequency range:	See table 8

7.7.1 HOW TO USE THE ABOVE FUNCTIONS

If CNTSEL is "L", the above functions((1)-(5))are valid. (CNTSEL is "H" or open, default values are valid.) After serial data are transferred, the data is latched by CNTSTB. Once, the data is latched, the above functions((1)-(5)) are effective.

If ADJSEL is "L", the above functions((6)-(7))are valid. (ADJSEL is "H" or open, default values are valid.) After serial data are transferred, the data is latched by CNTSTB2. Once, the data is latched, the above functions((6)-(7)) are effective.

Please keep CNTSTB/2 to be "L" during transferring data. Input data can be changed during power on, but LCD display may be disturbed. When the serial data are changed, we recommend that the backlight power is off using BRTC function.

Table 1. CNTDAT (Serial data) Composition

DATA	DATA name	Function	
D0	INT	Prohibit "0"	
D1	VEX4	Expansion mode	See table 2
D2	VEX3	Expansion mode	
D3	VEX2	Expansion mode	
D4	VEX1	Expansion mode	
D5	VEX0	Expansion mode	
D6	VD7	Vertical display position (MSB)	See table 3
D7	VD6	Vertical display position	
D8	VD5	Vertical display position	
D9	VD4	Vertical display position	
D10	VD3	Vertical display position	
D11	VD2	Vertical display position	
D12	VD1	Vertical display position	
D13	VD0	Vertical display position (LSB)	
D14	DELAY6	CLK delay (MSB)	See table 4
D15	DELAY5	CLK delay	
D16	DELAY4	CLK delay	
D17	DELAY3	CLK delay	
D18	DELAY2	CLK delay	
D19	DELAY1	CLK delay	
D20	DELAY0	CLK delay (LSB)	
D21	CKS	CLK signal	See table 5
D22	HD9	Horizontal display position (MSB)	See table 6
D23	HD8	Horizontal display position	
D24	HD7	Horizontal display position	
D25	HD6	Horizontal display position	
D26	HD5	Horizontal display position	
D27	HD4	Horizontal display position	
D28	HD3	Horizontal display position	
D29	HD2	Horizontal display position	
D30	HD1	Horizontal display position	
D31	HD0	Horizontal display position (LSB)	
D32	HSE11	CLK counts of horizontal period (MSB)	See table 7
D33	HSE10	CLK counts of horizontal period	
D34	HSE9	CLK counts of horizontal period	
D35	HSE8	CLK counts of horizontal period	
D36	HSE7	CLK counts of horizontal period	
D37	HSE6	CLK counts of horizontal period	
D38	HSE5	CLK counts of horizontal period	
D39	HSE4	CLK counts of horizontal period	
D40	HSE3	CLK counts of horizontal period	
D41	HSE2	CLK counts of horizontal period	
D42	HSE1	CLK counts of horizontal period	
D43	HSE0	CLK counts of horizontal period (LSB)	
D44	MOD2	CLK frequency select	See table 8
D45	MOD1	CLK frequency select	
D46	MOD0	CLK frequency select	

Table 1. CNTDAT Composition (continuation)

DATA	DATA name	Function	
AD0	DAD0	Color adjust data (LSB)	See table 9
AD1	DAD1	Color adjust data	
AD2	DAD2	Color adjust data	
AD3	DAD3	Color adjust data	
AD4	DAD4	Color adjust data	
AD5	DAD5	Color adjust data	
AD6	DAD6	Color adjust data	
AD7	DAD7	Color adjust data (MSB)	
AD8	DAA3	Color adjust select data (MSB)	See table 10
AD9	DAA2	Color adjust select data	
AD10	DAA1	Color adjust select data	
AD11	DAA0	Color adjust select data (LSB)	

Table 2. Expansion mode (VEX4 to VEX0 : 5bit)

VEX4	VEX3	VEX2	VEX1	VEX0	Vertical magnification	Display mode	Display image
0	0	0	0	0	1	UXGA	Standard Note 1
0	0	0	0	1	—	Prohibit	See 7.8.3 DISPLAY IMAGE
0	0	0	1	0	—	Prohibit	
0	0	0	1	1	2.0	SVGA	
0	0	1	0	0	2.5	VGA	
0	0	1	0	1	—	Prohibit	
0	0	1	1	0	—	Prohibit	
0	0	1	1	1	—	Prohibit	
0	1	0	0	0	—	Prohibit	
0	1	0	0	1	—	Prohibit	
0	1	0	1	0	—	Prohibit	
0	1	0	1	1	—	Prohibit	
0	1	1	0	0	1.17	SXGA	
0	1	1	0	1	1.38	1152 × 864(VESA)	
0	1	1	1	0	—	Prohibit	
0	1	1	1	1	1.56	XGA	
1	0	0	0	0	3.0	VGA-TEXT	
1	0	0	0	1	—	Prohibit	
1	0	0	1	0	—	Prohibit	
1	0	0	1	1	1.33	1152 × 900(SUN)	
1	0	1	0	0	—	Prohibit	
1	0	1	0	1	—	Prohibit	
1	0	1	1	0	1.92	832 × 624(MAC)	
1	0	1	1	1	—	Prohibit	
1	1	0	0	0	—	SUN	
1	1	0	0	1	—	Prohibit	
1	1	0	1	0	—	Prohibit	
1	1	0	1	1	—	Prohibit	
1	1	1	0	0	3.4	640 × 350(IBM)	
1	1	1	0	1	—	Prohibit	
1	1	1	1	0	—	Prohibit	
1	1	1	1	1	—	Prohibit	

Note 1: Display mode is UXGA, when CNTSEL is "H" or open".

Table 3. Vertical display position (VD7 to VD0 : 8bit)

VD7	VD6	VD5	VD4	VD3	VD2	VD1	VD0	Vertical position [H] note 1
0	0	0	0	0	0	0	0	Prohibit
0	0	0	0	0	0	0	1	Prohibit
0	0	0	0	0	0	1	0	Prohibit
0	0	0	0	0	0	1	1	Prohibit
0	0	0	0	0	1	0	0	4
0	0	0	0	0	1	0	1	5
·	·	·	·	·	·	·	·	·
·	·	·	·	·	·	·	·	·
·	·	·	·	·	·	·	·	·
1	1	1	1	1	1	0	1	253
1	1	1	1	1	1	1	0	254
1	1	1	1	1	1	1	1	255 note 2

Note 1: The number of horizontal line between Vsync-fall and RGB data valid.
Note 2: The maximum number is based on horizontal line count of the display mode.
Note 3: Vertical position is fixed at 49H, when CNTCEL is "H" or "open".

Table 4. CLK delay (DELAY6 to DELAY0 : 7bit)

DELAY[6..0]	Delay	Unit	DELAY[6..0]	Delay	Unit	DELAY[6..0]	Delay	Unit
00H	TBD	ns	30H	TBD	ns	60H	TBD	ns
01H	TBD	ns	31H	TBD	ns	61H	TBD	ns
02H	TBD	ns	32H	TBD	ns	62H	TBD	ns
03H	TBD	ns	33H	TBD	ns	63H	TBD	ns
04H	TBD	ns	34H	TBD	ns	64H	TBD	ns
05H	TBD	ns	35H	TBD	ns	65H	TBD	ns
06H	TBD	ns	36H	TBD	ns	66H	TBD	ns
07H	TBD	ns	37H	TBD	ns	67H	TBD	ns
08H	TBD	ns	38H	TBD	ns	68H	TBD	ns
09H	TBD	ns	39H	TBD	ns	69H	TBD	ns
0AH	TBD	ns	3AH	TBD	ns	6AH	TBD	ns
0BH	TBD	ns	3BH	TBD	ns	6BH	TBD	ns
0CH	TBD	ns	3CH	TBD	ns	6CH	TBD	ns
0DH	TBD	ns	3DH	TBD	ns	6DH	TBD	ns
0EH	TBD	ns	3EH	TBD	ns	6EH	TBD	ns
0FH	TBD	ns	3FH	TBD	ns	6FH	TBD	ns
10H	TBD	ns	40H	TBD	ns	70H	TBD	ns
11H	TBD	ns	41H	TBD	ns	71H	TBD	ns
12H	TBD	ns	42H	TBD	ns	72H	TBD	ns
13H	TBD	ns	43H	TBD	ns	73H	TBD	ns
14H	TBD	ns	44H	TBD	ns	74H	TBD	ns
15H	TBD	ns	45H	TBD	ns	75H	TBD	ns
16H	TBD	ns	46H	TBD	ns	76H	TBD	ns
17H	TBD	ns	47H	TBD	ns	77H	TBD	ns
18H	TBD	ns	48H	TBD	ns	78H	TBD	ns
19H	TBD	ns	49H	TBD	ns	79H	TBD	ns
1AH	TBD	ns	4AH	TBD	ns	7AH	TBD	ns
1BH	TBD	ns	4BH	TBD	ns	7BH	TBD	ns
1CH	TBD	ns	4CH	TBD	ns	7CH	TBD	ns
1DH	TBD	ns	4DH	TBD	ns	7DH	TBD	ns
1EH	TBD	ns	4EH	TBD	ns	7EH	TBD	ns
1FH	TBD	ns	4FH	TBD	ns	7FH	TBD	ns
20H	TBD	ns	50H	TBD	ns			
21H	TBD	ns	51H	TBD	ns			
22H	TBD	ns	52H	TBD	ns			
23H	TBD	ns	53H	TBD	ns			
24H	TBD	ns	54H	TBD	ns			
25H	TBD	ns	55H	TBD	ns			
26H	TBD	ns	56H	TBD	ns			
27H	TBD	ns	57H	TBD	ns			
28H	TBD	ns	58H	TBD	ns			
29H	TBD	ns	59H	TBD	ns			
2AH	TBD	ns	5AH	TBD	ns			
2BH	TBD	ns	5BH	TBD	ns			
2CH	TBD	ns	5CH	TBD	ns			
2DH	TBD	ns	5DH	TBD	ns			
2EH	TBD	ns	5EH	TBD	ns			
2FH	TBD	ns	5FH	TBD	ns			

Note 1: DELAY[6..0] is fixed at 00H, when CNTSEL is "H" or "open".

note 2: This delay value is typical value at Ta=25℃. And the value varies by the ambient temperature and the module itself.

Please set up a preferable display position. See the following references.

① Variation of CLK delay by temperature drift. (only reference) The temperature constant of CLK delay is 0.2%/℃.

Calculated example:

In case of delay time is 20ns at Ta=25℃;

(a) In case Ta rising to 50℃.

Increase of delay time → (50℃−25℃)×0.002×20ns=+1ns

So, the total delay time is 21 ns at Ta=50℃.

(b) In case Ta falling to 0℃.

Decrease of delay time → (0℃−25℃)×0.002×20ns=-1ns

So, the total delay time is 19 ns at Ta=0℃.

② Variation of CLK delay time against each LCD module. (only reference)

−10.5% to +14.4%

Table 5. CLK reverse signal

CKS	FUNCTION
0	DATA is sampled on rising edge of CLK. 
1	DATA is sampled on falling edge of CLK. 

Note 1: CKS is "0", when CNTSEL is "H" or "open".

Table 6. Horizontal display position (HD9 to HD0 : 10bit)

HD9	HD8	HD7	HD6	HD5	HD4	HD3	HD2	HD1	HD0	Horizontal position [CLK] Note 1
0	0	0	0	0	0	0	0	0	0	Prohibit
0	0	0	0	0	0	0	0	0	1	Prohibit
·	·	·	·	·	·	·	·	·	·	·
·	·	·	·	·	·	·	·	·	·	·
0	0	0	0	1	1	1	1	1	1	Prohibit
0	0	0	1	0	0	0	0	0	0	64
0	0	0	1	0	0	0	0	0	1	65
·	·	·	·	·	·	·	·	·	·	·
·	·	·	·	·	·	·	·	·	·	·
1	1	1	1	1	1	1	1	0	1	1021
1	1	1	1	1	1	1	1	1	0	1022
1	1	1	1	1	1	1	1	1	1	1023

Note 1: The number of CLK between Hsync-fall and RGB data valid.

Note 2: Horizontal position is set at 496 CLK, when CNTSET is "H" or "open".

Table 7. CLK counts of horizontal period (HSE11 to HSE0 : 12bit)

HSE11	HSE10	HSE9	HSE8	HSE7	HSE6	HSE5	HSE4	HSE3	HSE2	HSE1	HSE0	CLK count Note 1
0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	1	1
.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	1	1	1	0	1	4093
1	1	1	1	1	1	1	1	1	1	1	0	4094
1	1	1	1	1	1	1	1	1	1	1	1	4095

Note 1: The number of CLK between Hsync signals.
Note 2: CLK number is set 2160 CLK, when CNTSEL is "H" or "open".
Note 3: If setting value is different from actual input signal, it may cause to malfunction.

Table 8. CLK frequency select (MOD2 to MOD0 : 3bit)

MOD2	MOD1	MOD0	CLK frequency [MHz]
0	0	0	Prohibit
0	0	1	Prohibit
0	1	0	140 to 170
0	1	1	110 to 140
1	0	0	80 to 110
1	0	1	70 to 80
1	1	0	60 to 70
1	1	1	50 to 60

Note 1: Set complying with input CLK frequency.
Note 2: CLK frequency is set 140 to 170 MHz, when CNTSEL is "H" or "open".

Table 9. Color control data (DAD7 to DAD0 : 8bit)

DAD7	DAD6	DAD5	DAD4	DAD3	DAD2	DAD1	DAD0	Adjusting value
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
0	1	1	1	1	1	1	1	127
1	0	0	0	0	0	0	0	128
1	0	0	0	0	0	0	1	129
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	0	1	253
1	1	1	1	1	1	1	0	254
1	1	1	1	1	1	1	1	255

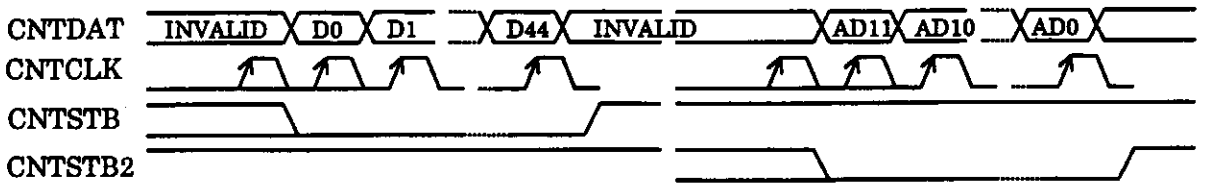
Note 1: Adjust value for selecting function above table.10.
Note 2: Different D/A-range depends on function selected.
Note 3: See more detail 7.8.4. COLOR CONTROL FUNCTIONS AND GRAPH IMAGES.

Table 10. Color adjust select data (DAA3 to DAA0 : 4bit)

DAA3	DAA2	DAA1	DAA0	Function
0	0	0	0	Prohibit
0	0	0	1	Prohibit
0	0	1	0	Prohibit
0	0	1	1	Prohibit
0	1	0	0	Sub-contrast R
0	1	0	1	Sub-contrast G
0	1	1	0	Sub-contrast B
0	1	1	1	Sub-brightness R
1	0	0	0	Sub-brightness G
1	0	0	1	Sub-brightness B
1	0	1	0	Prohibit
1	0	1	1	Prohibit
1	1	0	0	Prohibit
1	1	0	1	Prohibit
1	1	1	0	Prohibit
1	1	1	1	Prohibit

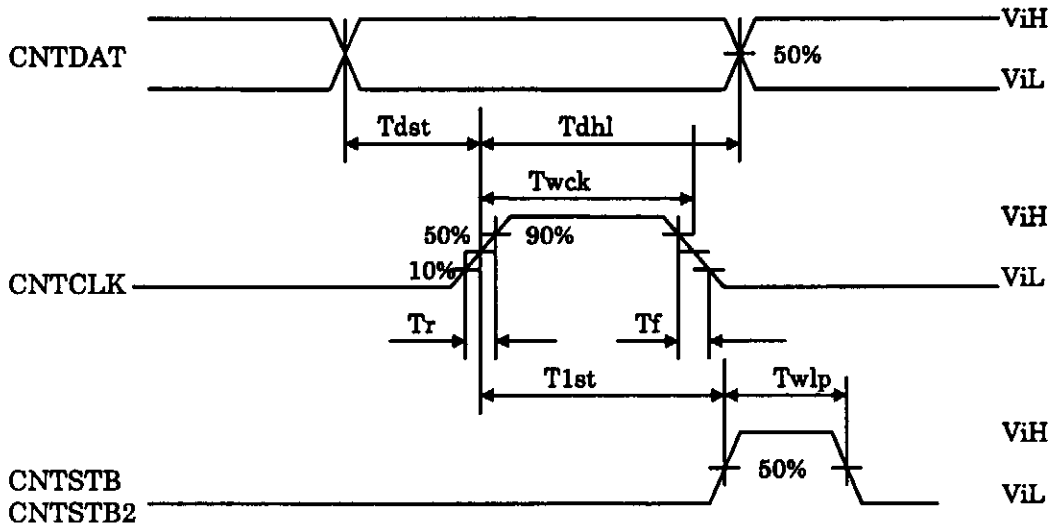
Note 1: See more detail 7.8.4. COLOR CONTROL FUNCTIONS AND GRAPH IMAGES.

7.7.2 SERIAL COMMUNICATION TIMINGS



Parameter	Symbol	Min.	Max.	Unit	Remark
CLK pulse-width	Twck	50	–	ns	CNTCLK
CLK frequency	Fclk	–	5	MHz	
DATA set-up-time	Tdst	50	–	ns	CNTDAT
DATA hold-time	Tdhl	50	–	ns	
Latch pulse-width	Twlp	50	–	ns	CNTSTB, CNTSTB2
Latch set-up-time	T1st	50	–	ns	
Rise / fall time	Tr , Tf	–	50	ns	CNT xxx

SERIAL COMMUNICATION WAVEFORM



7.8 EXPANSION FUNCTIONS

7.8.1 HOW TO USE EXPANSION MODES

Expansion mode is a function to expand screen. For example, VGA signal has 640 × 480 pixels. But, if the display data can expanded to 2.5 times vertically and horizontally, VGA screen image can be displayed fully on the screen of UXGA resolution.

This LCD module has the function that expands vertical direction as shown in Table 1. And expanding horizontal direction is possible by setting input CLK frequency equivalent to the magnification. It is necessary to make this CLK outside of this LCD module.

Please adopt this mode after evaluating display quality, because the appearance in expansion mode is happened to be relatively bad in some cases.

The followings show display magnifications for each mode.

Input display	Number of pixels	Magnification	
		Vertical	Horizontal note 1
UXGA	1600 x 1200	1.0	1.0
SXGA	1280 x 1024	1.17	1.25
XGA	1152 x 864	1.38	1.38
	1024 x 768	1.56	1.56
SUN	1152 x 900	1.33	1.38
MAC	832 x 624	1.92	1.92
SVGA	800 x 600	2.0	2.0
VGA	640 x 480	2.5	2.5
VGA text	720 x 400	3.0	2.5
IBM VGA	640 x 350	3.4	2.5

note 1: The horizontal magnification multiples the input clock(CLK).

Input CLK = system CLK × horizontal magnification

Example: In case of UXGA and VGA, CLK frequency can be decided as follows.

UXGA: System CLK(162.0MHz) × 1.0=162.0MHz

VGA : System CLK(25.175MHz) × 2.5= 62.94MHz

7.8.2 SETTING SERIAL DATA FOR EXPANSION

Input signal								Module serial-data setting		
Mode	System CLK [MHz]	Hsync [kHz]	Vsync [Hz]	Horizontal		Vertical		HSE	HD	VD
				Count Number [CLK]	DSP [CLK]	Count Number [H]	DSP [H]	Calculation formula		
				(A)	(B)	—	(C)	(A)x Ver.magni	(B)x Hor.magni	=(C)
UXGA (1600 x1200)	162.0	75.000	60.000	2160	496	1250	49	(A) x 1	(B) x 1	
SXGA (1280 x1024)	108.0*	63.981	60.02	1688	360	1066	41	(A) x 1.25	(B) x 1.25	
	117.0*	71.691	67.189	1632	336	1067	41			
	125.0*	75.120	71.204	1664	352	1055	28			
	130.076*	76.968	72.000	1690	378	1069	42			
	135.0*	78.125	72.005	1728	384	1085	58			
	135.0*	79.976	75.025	1688	392	1066	41			
SUN (1152 x 900)	94.500*	61.845	66.003	1528	336	937	35	(A) x 1.38	(B) x 1.38	
XGA (1024 x 768)	65*	48.363	60.004	1344	296	806	35	(A) x 1.56	(B) x 1.56	
	75*	56.476	70.069	1328	280	806	35			
	78.75*	60.023	75.029	1312	272	800	31			
XGA (1152 x 864)	94.5*	64.198	70.239	1472	288	914	49	(A) x 1.56	(B) x 1.56	
	108.0*	67.500	75.000	1600	384	900	35			
MAC (832x624)	57.283*	49.725	74.5	1152	288	667	42	(A)x1.92	(B)x1.92	
SVGA (800 x 600)	36*	35.156	56.25	1024	200	625	24	(A) x 2.0	(B) x 2.0	
	40*	37.879	60.317	1056	216	628	27			
	50*	48.077	72.188	1040	184	666	29			
	49.5*	46.875	75	1056	240	666	24			
VGA (640 x 480)	25.175*	31.469	59.94	800	144	525	35	(A) x 2.5	(B) x 2.5	
	31.5*	37.861	72.809	832	168	520	31			
	31.5*	37.5	75	840	184	500	19			
	30.24*	35.0	66.667	864	160	525	42			
VGA text (720 x 400)	28.322*	31.469	70.087	900	153	449	37	(A) x 2.2	(B) x 2.2	
IBM VGA (640 x 350)	25.175*	31.469	70.087	800	144	449	62	(A) x 2.5	(B) x 2.5	

*: Standard timings (Please set them up properly for correct expansion.

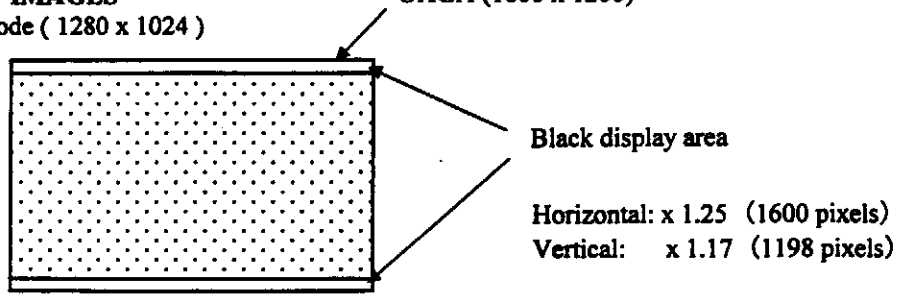
Note 1: DSP = Display Start Period. DSP is total of "pulse-width" and "back-porch".

Note 2: HD and VD are approximate value. Set HD and VD in case of adjusting display to the screen center.

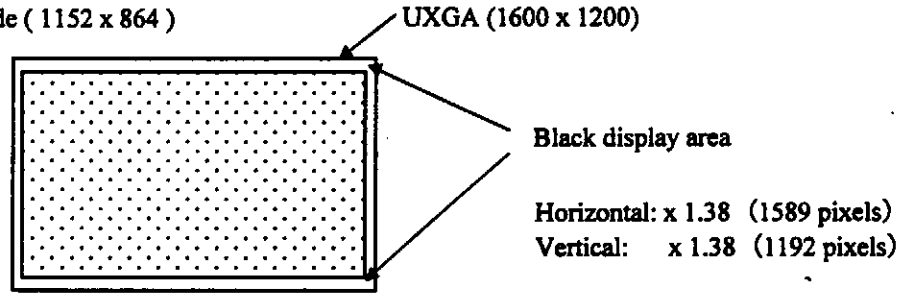
Note 3: The pulse-width of Hsync, Vsync and Back-porch are the same as UXGA-mode (Standard-mode).

7.8.3 DISPLAY IMAGES

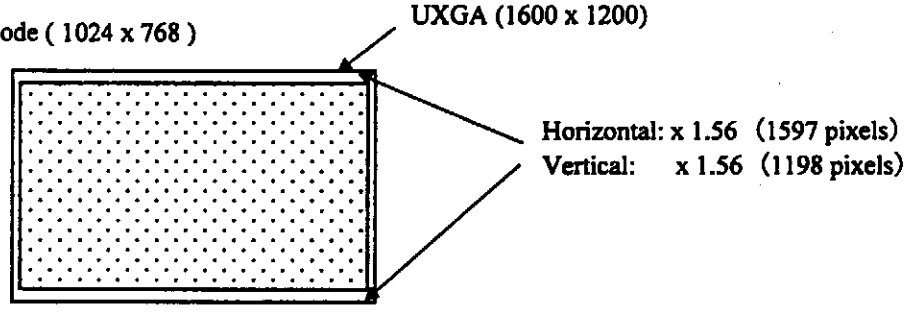
1) SXGA mode (1280 x 1024)



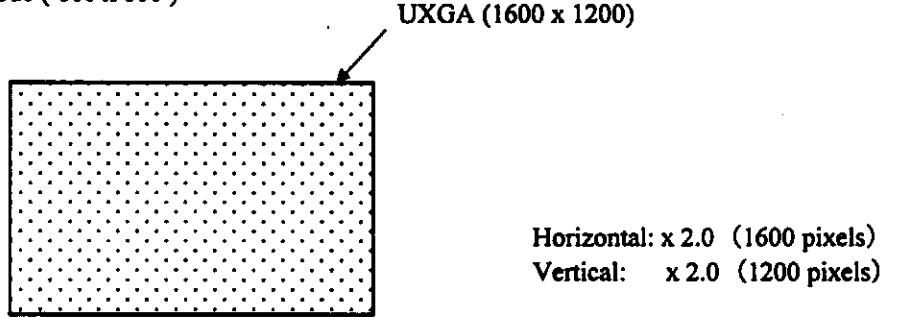
2) XGA mode (1152 x 864)



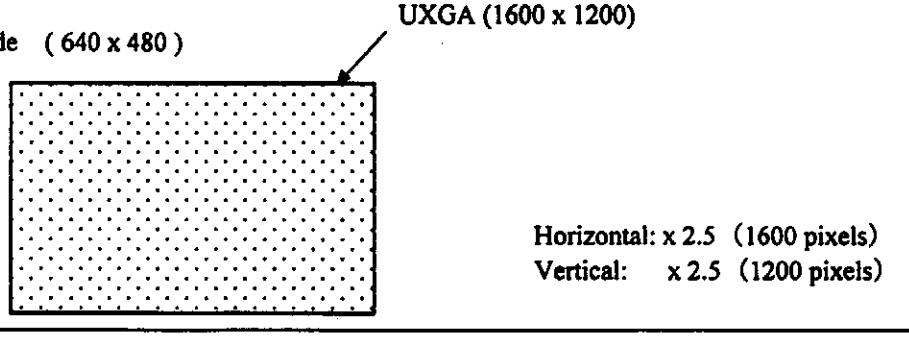
XGA mode (1024 x 768)



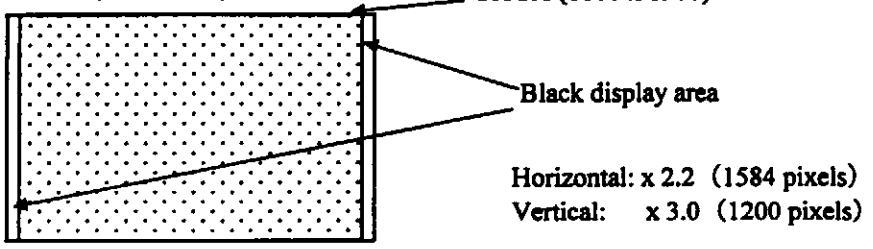
3) SVGA mode (800 x 600)



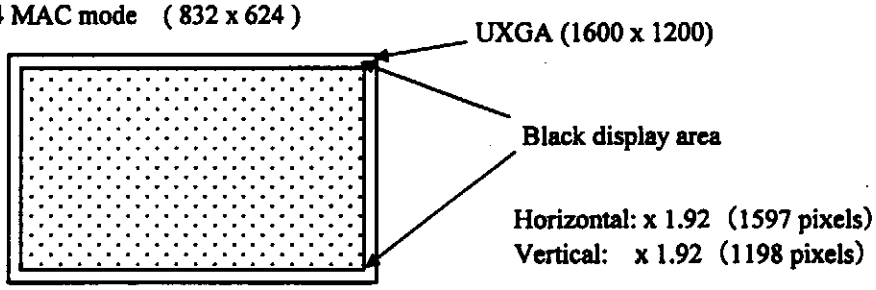
4) VGA mode (640 x 480)



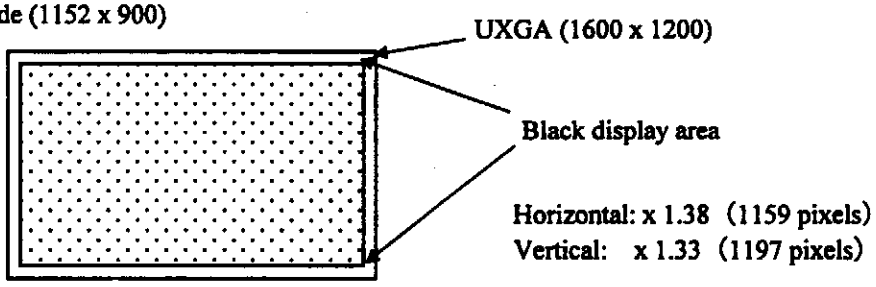
5) VGA text mode (720 x 400)



6) 832 x 624 MAC mode (832 x 624)



7) SUN mode (1152 x 900)



7.8.4 COLOR CONTROL FUNCTIONS AND GRAPHIC IMAGE

This LCD module can adjust the following functions by serial data input (table.1)

(1) Sub-contrast each R,G,B:
(2) Sub-brightness each R,G,B:

} See table 9, 10 and **7.8.4 COLOR CONTROL FUNCTION AND GRAPH IMAGE**

(1) Sub-contrast R,G,B

Sub-contrast can adjust each R/G/B with controlling the amplitude of input video signal.

Default value: 128, Valid range: 78 to 198
Contrast minimum: 78
Contrast maximum: 198
ADJSEL="H" or "Open" : Default value=128

(2) Sub-brightness R,G,B

Sub-brightness can adjust each R/G/B with adjusting the black level of input video signal.

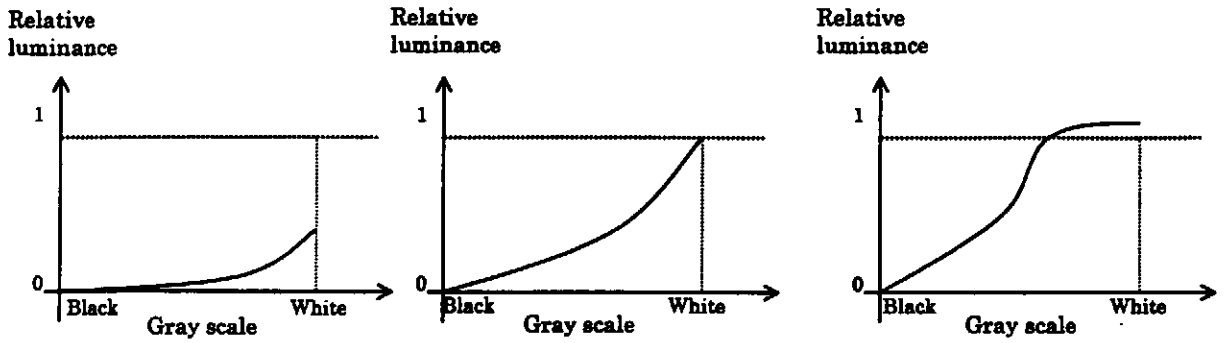
Default value: 128, Valid range: 55 to 163
Brightness minimum: 163
Brightness maximum: 55
ADJSEL="H" or "Open" : Default value=128

Note1: If the values is go over above valid range, LCD module will not be destroy. However LCD will be inferiority. Please keep values within the valid range.

Note2: Although set up the same values are set up for each LCDs, each LCD color might be slightly ill be different. And also, will be afraid to deviate values from optical characteristics. Please adopt this functions evaluating display quality.

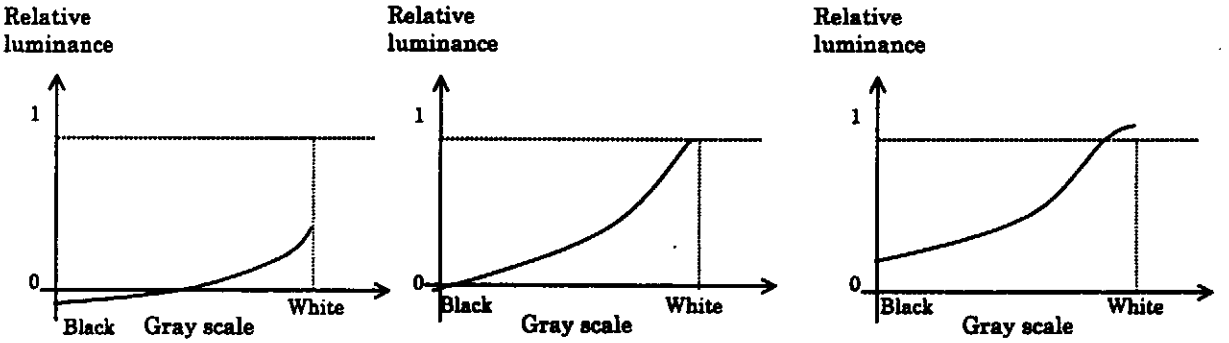
《GRAPH IMAGE》

・Sub contrast



Sub contrast
Min value ◄——— DEFAULT ———► Max value

・Sub brightness



Sub brightness
Min value ◄——— DEFAULT ———► Max value

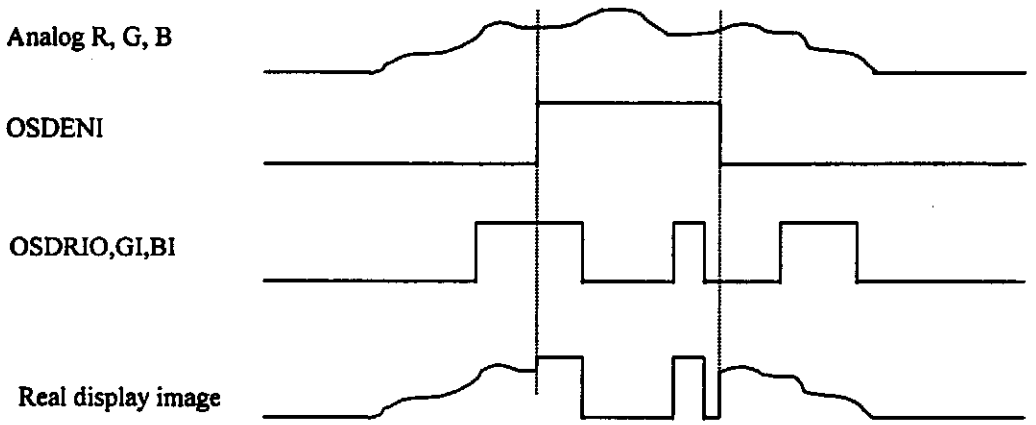
7.9 OSD FUNCTIONS

OSD (On Screen Display) is the function to display the other digital data on the input analog valid data. Possible to display 1 bit data for each R/G/B color (8 colors). OSD function is valid for the period of OSDENI

OSDRI, OSDGI, OSDBI: digital data for OSD
OSDENI="H": OSD signal is valid
OSDENI="L": OSD signal is not valid

OSD is the sub-display for function-control and the display quality will not be guaranteed. Please adopt the OSD image evaluating display quality.

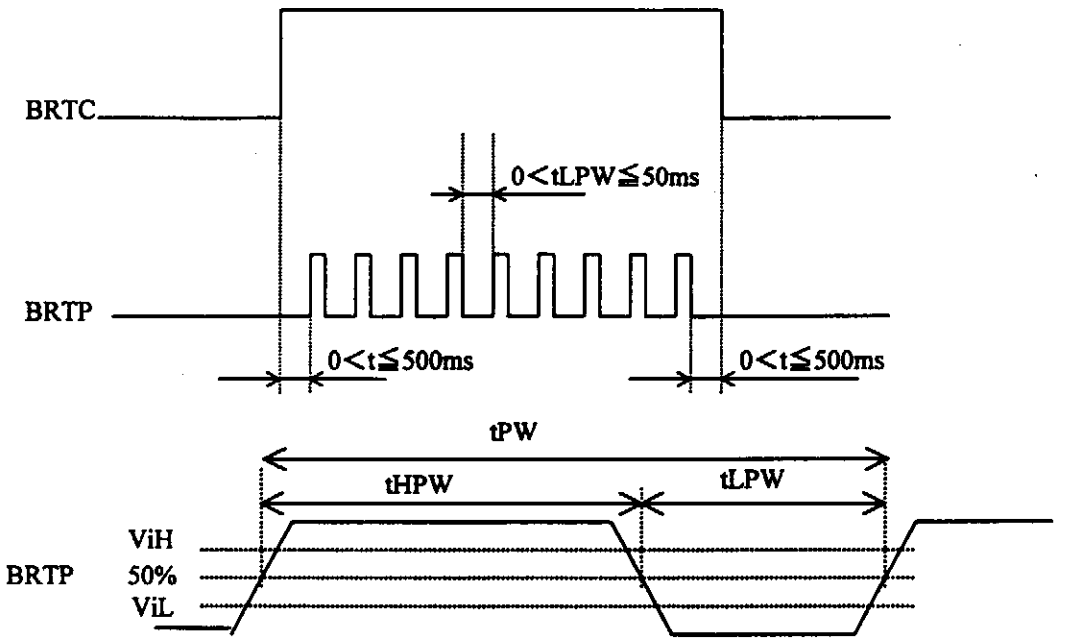
《OSD image》



7.10 OUTSIDE CONTROL FOR LUMINANCE

Outside control is valid, when PWSEL="L" and input signal for BRTP. Luminance can be controlled by the duty value of input signal for BRTP.
Duty=100%: luminance is maximum.
Duty=20%: luminance is minimum.

Timing for BRTP



Parameters	Symbols	Min.	Typ.	Max.	Unit	Remarks
Frequency	1/tPW	185	–	325	Hz	–
"L" period	tLPW	–	–	50	ms	
Pulse-width	tHPW/tPW	20	–	100	%	at max. luminance (100%)
Input voltage	ViL	0	–	0.8	V	–
	ViH	2.0	–	5.0	V	–

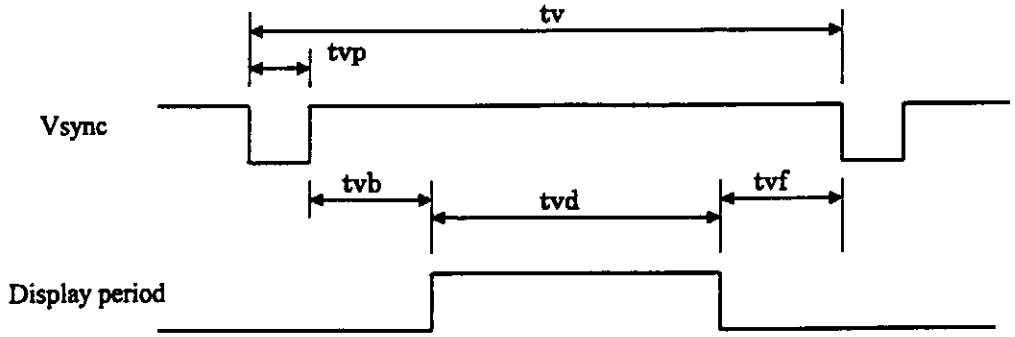
Regarding set up for frequency, refer to the below method.
Set up frequency = Vsync frequency × (n+0.25) or (n+0.75)
Adopt the frequency evaluating the display quality, because the display will be disturbed depend on frequency.

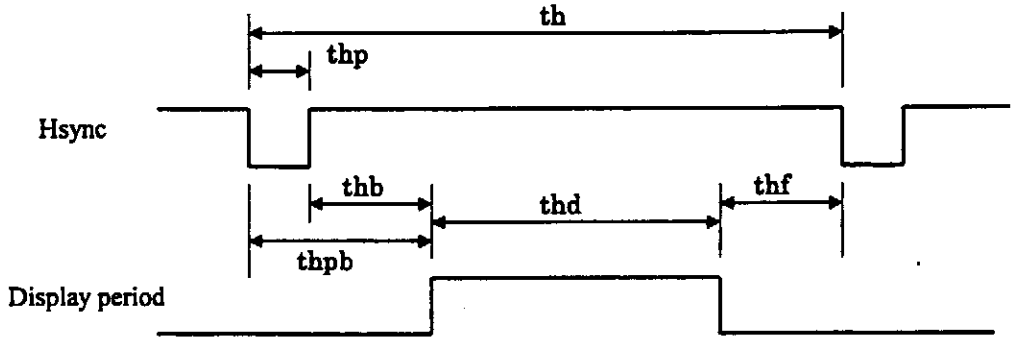
7.11 INPUT SIGNAL TIMINGS

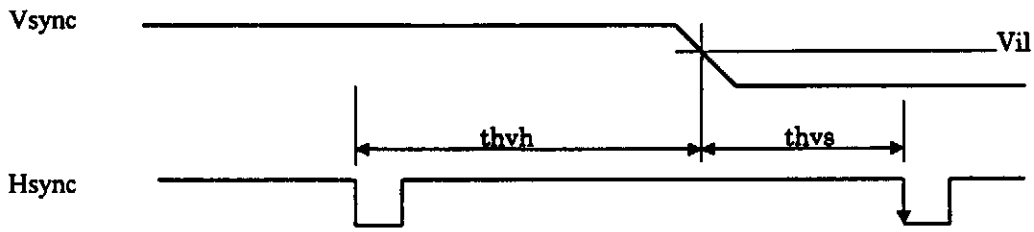
7.11.1 UXGA MODE (STANDARD)

Name		Symbols	Min.	Typ.	Max.	Unit	Remarks
CLK	Frequency	1/tc	– –	162.0 6.17	169.0 –	MHz ns	UXGA standard
	Rise / Fall	tcrf	–	–	0.5	ns	–
	Pulse-width	tc / tcl	0.4	0.5	0.6	–	–
Hsync	Period	th	12.3 –	13.333 2160	17.0 –	μs CLK	75.0kHz (typ.)
	Display	thd	– –	9.877 1600	– –	μs CLK	–
	Front-porch	thf	– 10	0.395 64	– –	μs CLK	–
	Pulse-width	thp	– 16	1.185 192	– –	μs CLK	–
	Back-porch	thb	1.0 94	1.877 304	– –	μs CLK	Note 1
	Pulse-width +Back-porch	thbp	1.8	–	–	μs	–
	V-Hsync timing hold/setup time	thvh	3	–	–	ns	–
		thvs	1	–	–	CLK	–
	Rise / Fall	thrf	–	–	10	ns	–
Vsync	Period	tv	133 –	16.667 1250	18.5 –	ms H	60.00Hz (typ.)
	Display	tvd	– –	16.000 1200	– –	ms H	–
	Front-porch	tvf	– 1	0.013 1	– –	ms H	–
	Pulse-width	tvp	– 2	0.040 3	– –	ms H	–
	Back-porch	tvb	– 5	0.613 46	– –	ms H	–

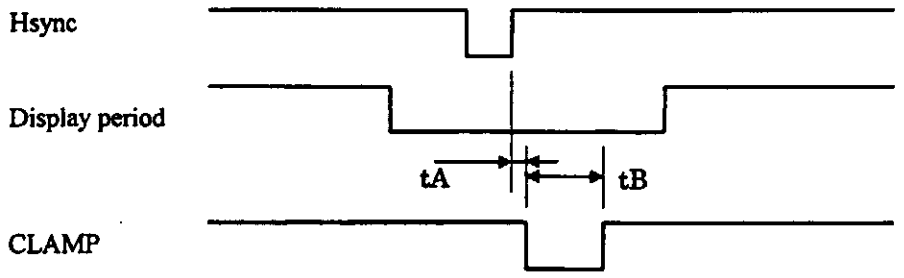
Note 1: Minimum value of Back-porch (thb) must be satisfied with both 1.0 μs and 44 CLK.


tv
tvp
Vsync
tvb
tvd
tvf
Display period


th
thp
Hsync
thb
thd
thf
thpb
Display period


Vsync
Vil
thvh
thvs
Hsync

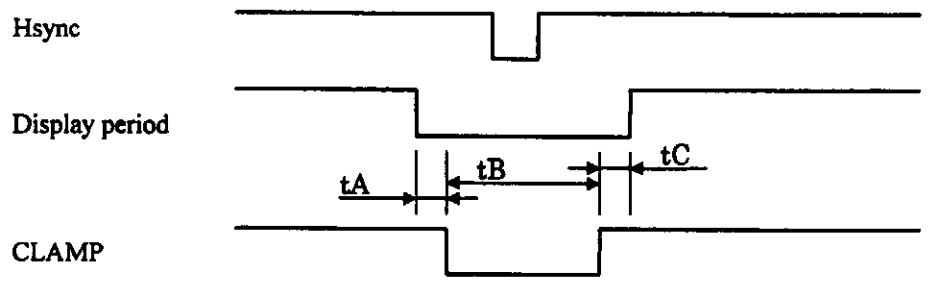
7.11.2 TIMING FOR GENERATING CLAMP SIGNAL INTERNALLY



MOD2	MOD1	MOD2	tA [CLK]	tB[CLK]
0	0	0	2	69
0	0	1		60
0	1	0		51
0	1	1		42
1	0	0		33
1	0	1		24
1	1	0		21
1	1	1		18

note 1: Exclude noises on analog R, G, B signals, because analog R, G, B signals are the black level reference during CLAMP="L". If noises are on the analog signals, luminance level of display is changed and the display becomes bad.

7.11.3 TIMING FOR INPUTTING CLAMP SIGNAL FROM OUTSIDE

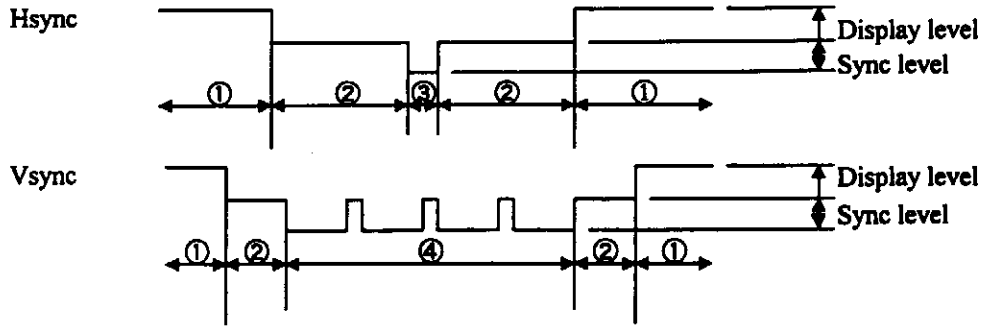


Items	Min.	Typ.	Max.	Unit	Remarks
tA	0.1	–	–	μs	–
tB	0.3	–	–	μs	–
tC	0.2	–	–	μs	–

note 1: Exclude noises on analog R, G, B signals, because analog R, G, B signals are the black level reference during CLAMP="L". If noises are on the analog signals, luminance level of display is changed and the display becomes bad.

note 2 : Attention for using Sync On Green signal
Clamp signals must be input during black level period as next page.
If Clamp signals are input during other period, the display becomes un-uniformity.

Sync on Green Input signal timings



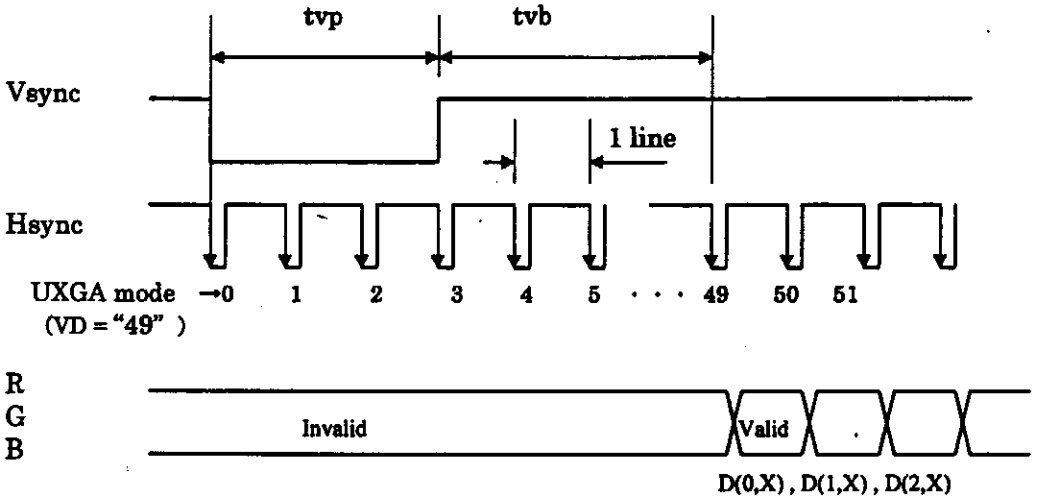
①:Display period ②:Black level period ③:Hsync period ④:Vsync period

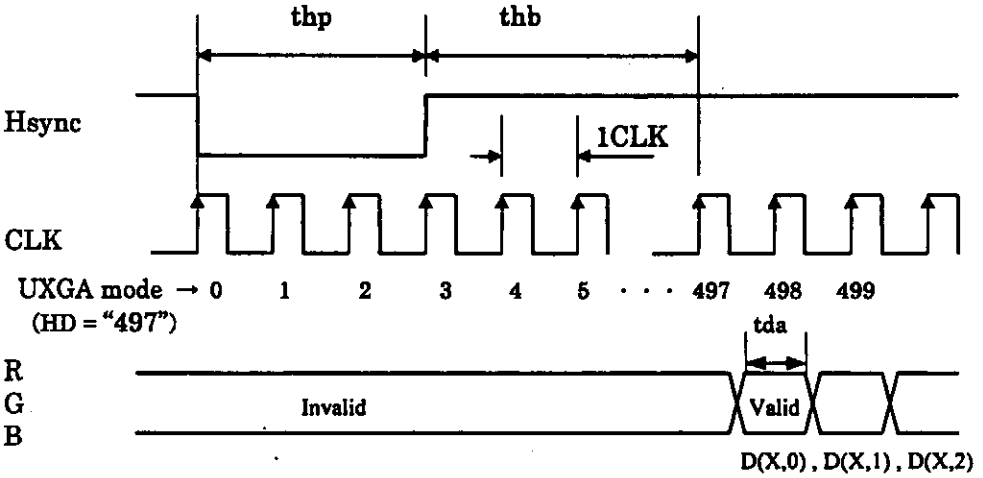
7.12 INPUT SIGNAL AND DISPLAY POSITIONS

7.12.1 UXGA STANDARD TIMINGS

Pixels

D(0,0)	D(0,1)	D(0,2)	. . . . .	D(0.1599)
D(1,0)	D(1,1)	D(1,2)	. . . . .	D(1,1599)
D(2,0)	D(2,1)	D(2,2)	. . . . .	D(2,1599)
.	.	.		.
.	.	.		.
.	.	.		.
.	.	.		.
D(1199,0)	D(1199,1)	D(1199,2)	. . . . .	D(1199,1599)





note 1: The tda should be more than 4ns

7.13 OPTICAL CHARACTERISTICS

(Ta = 25℃, VDD = 12V, VDDB = 12V)

Items	Symbols	Condition	Min.	Typ.	Max.	Unit	Remarks
Contrast ratio	CR	γ=2.2 viewing angle θR=0°, θL=0°, θD=0°, White/Black, at center	100	250	-	-	note 1
Luminance	Lvmax	White, at center	150	200	-	cd/m^2	note 2
Luminance uniformity	—	White	-	1.10	1.30	-	note 3

Reference data

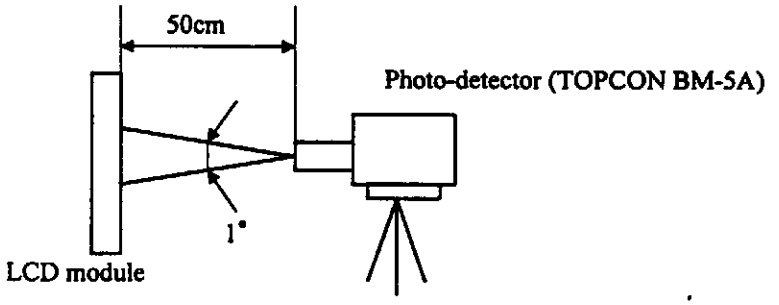
(Ta = 25℃, VDD = 12V, VDDB = 12V)

Items	Symbols	Condition	Min.	Typ.	Max.	Unit	Remarks
Chromaticity Coordinates	C	θR=0°, θL=0°,θU=0°, θD=0°, at center, to NTSC	50	60	-	%	-
	W	White (x, y)	-	TBD	-	-	-
	R	Red (x, y)	-	TBD	-	-	-
	G	Green (x, y)	-	TBD	-	-	-
	B	Blue (x, y)	-	TBD	-	-	-
Viewing angle range	θR	CR > 10, θU=0°, θD=0°	70	85	-	deg.	Note 4
	θL		70	85	-	deg.	
	θU	CR > 10, θR=0°, θL=0°	70	85	-	deg.	
	θD		70	85	-	deg.	
Viewing angle range	θR	CR > 5, θU=0°, θD=0°	85	-	-	deg.	
	θL		85	-	-	deg.	
	θU	CR > 5, θR=0°, θL=0°	85	-	-	deg.	
	θD		85	-	-	deg.	
Response time	Ton	Black to White	-	40	-	ms	note 5
	Toff	White to Black	-	20	-		
Luminance control range	—	Maximum luminance (100%)	-	30—100	-	%	-

note 1: The contrast ratio is calculated by using the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance with all pixels in "white"}}{\text{Luminance with all pixels in "black"}}$$

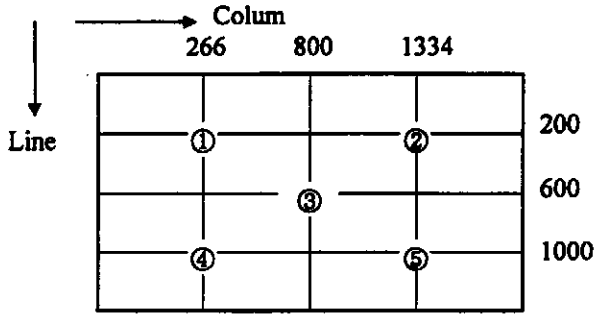
note 2: The luminance is measured after 20 minutes from the module works, with all pixels in "white". The typical value is measured after luminance saturation.
Display mode: VESA UXGA-60Hz
RGB input voltage: 0.7Vp-p
Contrast: Default



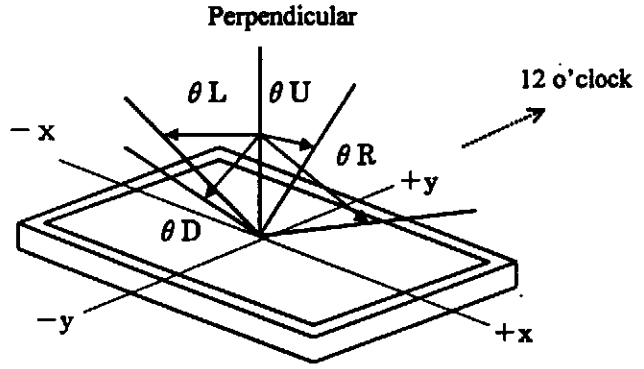
note 3: Luminance uniformity is calculated by using the following formula.

$$\text{Luminance uniformity} = \frac{\text{Maximum luminance}}{\text{Minimum luminance}}$$

The luminance is measured at near the five points shown below.

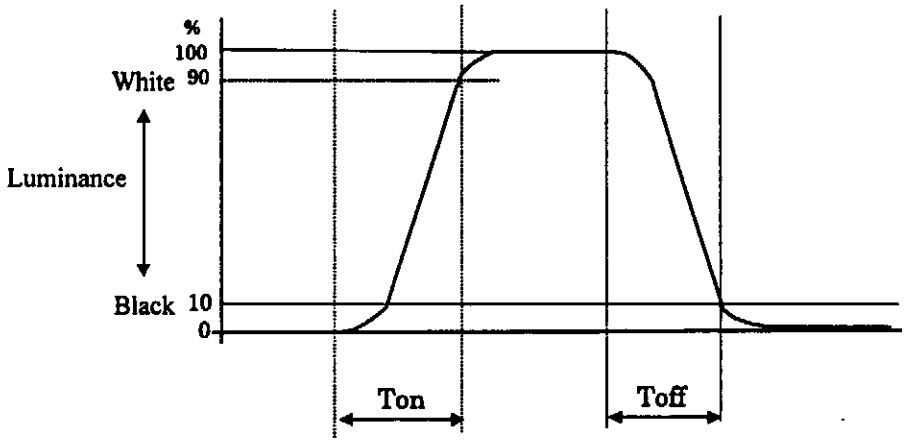


note 4: Definitions of viewing angle are as follows.



note 5: Definitions of response time is as follows.

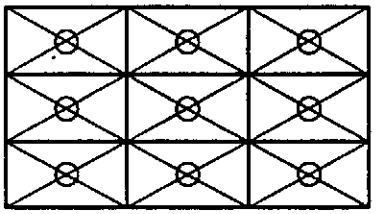
Photo-detector out put signal is measured when the luminance changes "black" to "white". Response time is the time between 0% and 90% of the photo-detector output amplitude.



7.14 RELIABILITY TEST

Test items	Test condition	Judgment
High temperature/humidity operation	50±2℃, 85% relative humidity 240 hours, Display data is black.	*1
Heat cycle (operation)	① 0℃±3℃···1 hour 55℃±3℃···1 hour ② 50 cycles , 4 hours/cycle ③ Display data is black.	*1
Thermal shock (non-operation)	① -20℃±3℃···30 minutes 60℃±3℃···30 minutes ② 100 cycles ③ Temperature transition time is within 5 minutes.	*1
Vibration (non-operation)	① 5-100Hz, 1.2G 1 minute/cycle, X,Y,Z direction ② 10 times each direction	*1, *2
Mechanical shock (non-operation)	① 30G, 11ms X,Y,Z direction ② 3 times each direction	*1, *2
ESD (operation)	150pF, 150Ω, ±10KV 9 places on a panel *3 10 times each place at one-second intervals	*1
Dust (operation)	15 kinds of dust (JIS-Z 8901) Hourly 15 seconds stir, 8 times repeat	*1

*1: Display function is checked by the same condition as LCD module out-going inspection.
*2: Physical damage
*3: Discharge points are shown in the figure.



7.15 EXPECTED LIFE-TIME OF THE LAMP

	Backlight
Condition	Luminance Maximum Room temp. (25±2℃) , Continuous operation
Expected value	50,000H
Criteria	Half value luminance (compared with initial value.)

Note 1: The lifetime is expected value (reference).
Note 2: This module consists of twelve lamps. Even though a lamp goes off, the other lamps may go off.

8. GENERAL CAUTIONS

Because next figures and sentences are very important, please understand these contents as follows.

⚠CAUTION	This figure is a mark that you will get hurt and/or the module will have damages when you make a mistake to operate.

	This figure is a mark that you will get electric shock when you make a mistake to operate.
	This figure is a mark that you will get hurt when you make a mistake to operate.

 **CAUTIONS**

Do not touch an inverter –on which a caution label is stucked– while the LCD module is working, because of dangerous high voltage.

(1) Caution when taking out the module

① Pick the pouch only, when in taking out the module from the carrier box.

(2) Cautions for handling the module

① As the electrostatic discharges may break the LCD module, handle the LCD module with care against electrostatic discharges.

②

 As the LCD panel and backlight element are made from fragile glass material, impulse and pressure to the LCD module should be avoided.

③ As the surface of polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.

④ Do not pull the interface connectors in or out while the LCD module is operating.

⑤ Put the module display side down on a flat horizontal plane.

⑥ Handle connectors and cables with care.

⑦ When the module is operating, do not lose CLK, Hsync, or Vsync signal. If any one or more of these signals is lost, the LCD panel would be damaged.

⑧ Do not put front side (display surface side) of the module on a desk or a table for a long time, because the display may become un-uniformity.

⑨ Don't push or rub the surface of LCD module.
If you do the scratches or the rubbing marks may left on the surface of the module.

⑩ The torque for mounting screw should never exceed 0.392 N·m (4kgf·cm)

(3) Cautions for the atmosphere

①Dew drop atmosphere must be avoided.

②Do not store and/or operate the LCD module in high temperature and/or high humidity atmosphere. Storage in an Electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.

③This module uses cold cathode fluorescent lamps. Therefore, the life-time of lamps becomes short conspicuously at low temperature.

④Do not operate the LCD module in high magnetic field.

(4) Cautions for the module characteristics

① Do not apply any fixed patterns data signal for a long time to the LCD module. It may cause image sticking. Use screen savers if the display pattern is fixed more than 30 minutes.

② The noise from the inverter circuit may be observed in the luminance control mode. This is neither defects nor malfunctions.

(5) Other cautions

① Do not disassemble and/or reassemble LCD module.

② Do not readjust variable resistors nor switches etc.

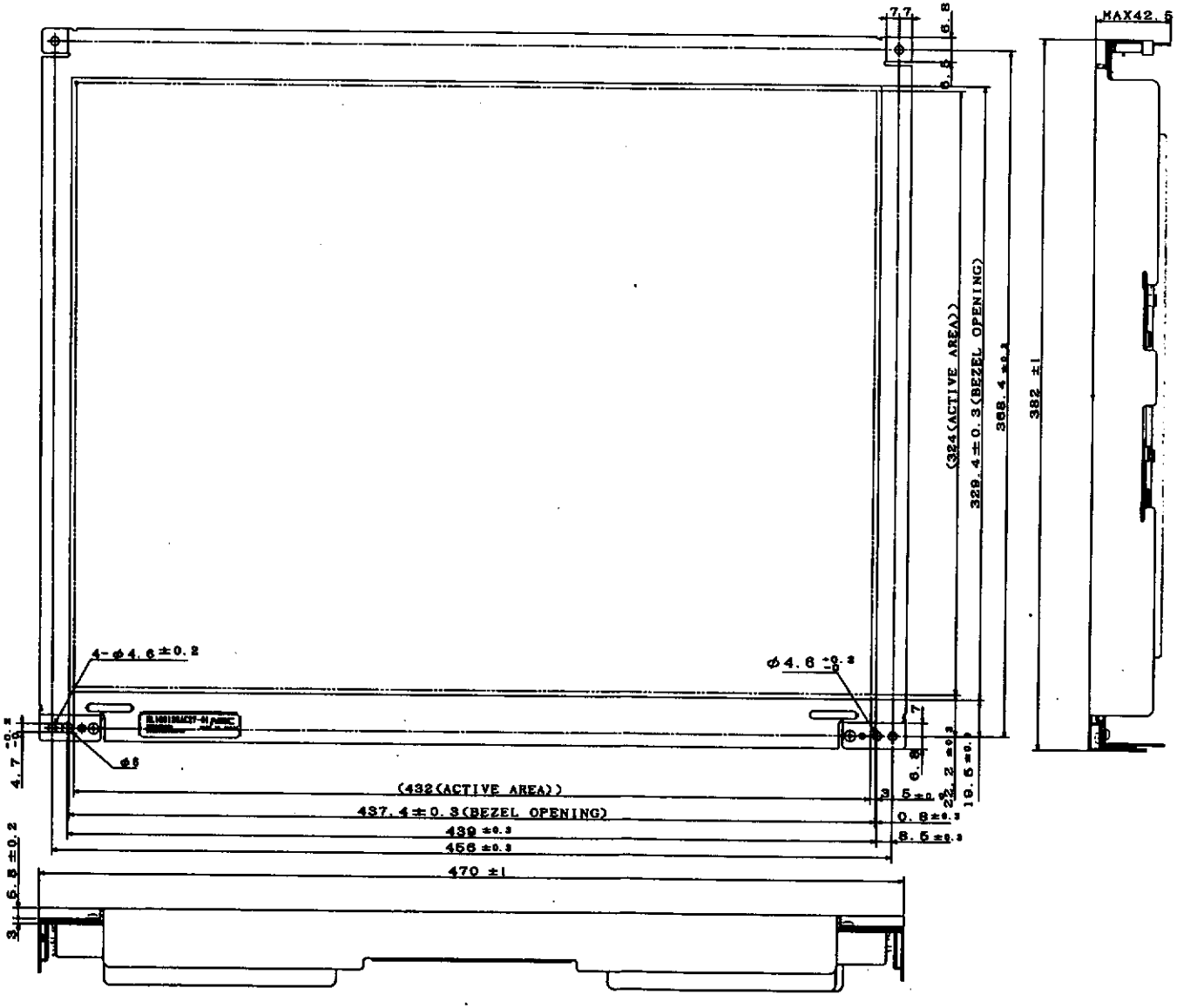
③ When returning the module for repair or etc., pack the module not to be broken. We recommend the original shipping packages.

Liquid Crystal Display has the following specific characteristics. There are not defects nor malfunctions.

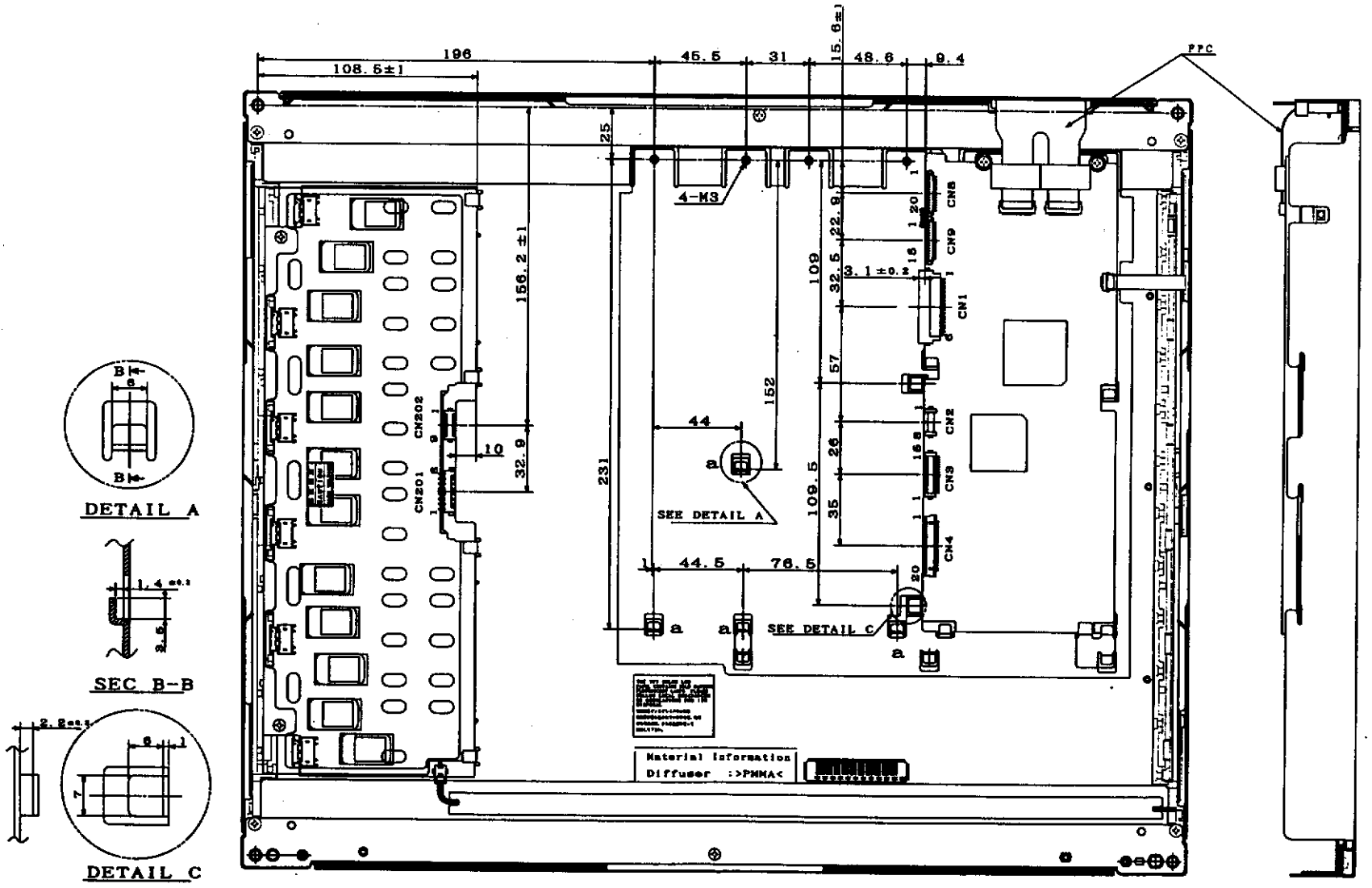
The ambient temperature may affect the display condition of LCD module.
The LCD module uses cold cathode tube for backlight. Optical characteristics, like luminance or uniformity, will change during time.

Uneven brightness and/or small spots may be noticed depending on different display patterns.

9.OUTLINE DRAWINGS
9.1 FRONT VIEW



9.2 REAR VIEW



DETAIL A

SEC B-B

DETAIL C

※ The torque for mounting screw should never exceed 0.392 N·m (4 kgf·cm).
※ Not shown tolerance of the dimensions are ±0.5 mm.

Revision History

Rev.	Prepared date	Revision contents	Approved	Checked	Prepared	Issued date
1	Sep. 3, 1999	No. DOD-H-7390		T. Kusanagi	Y. Okuda	-